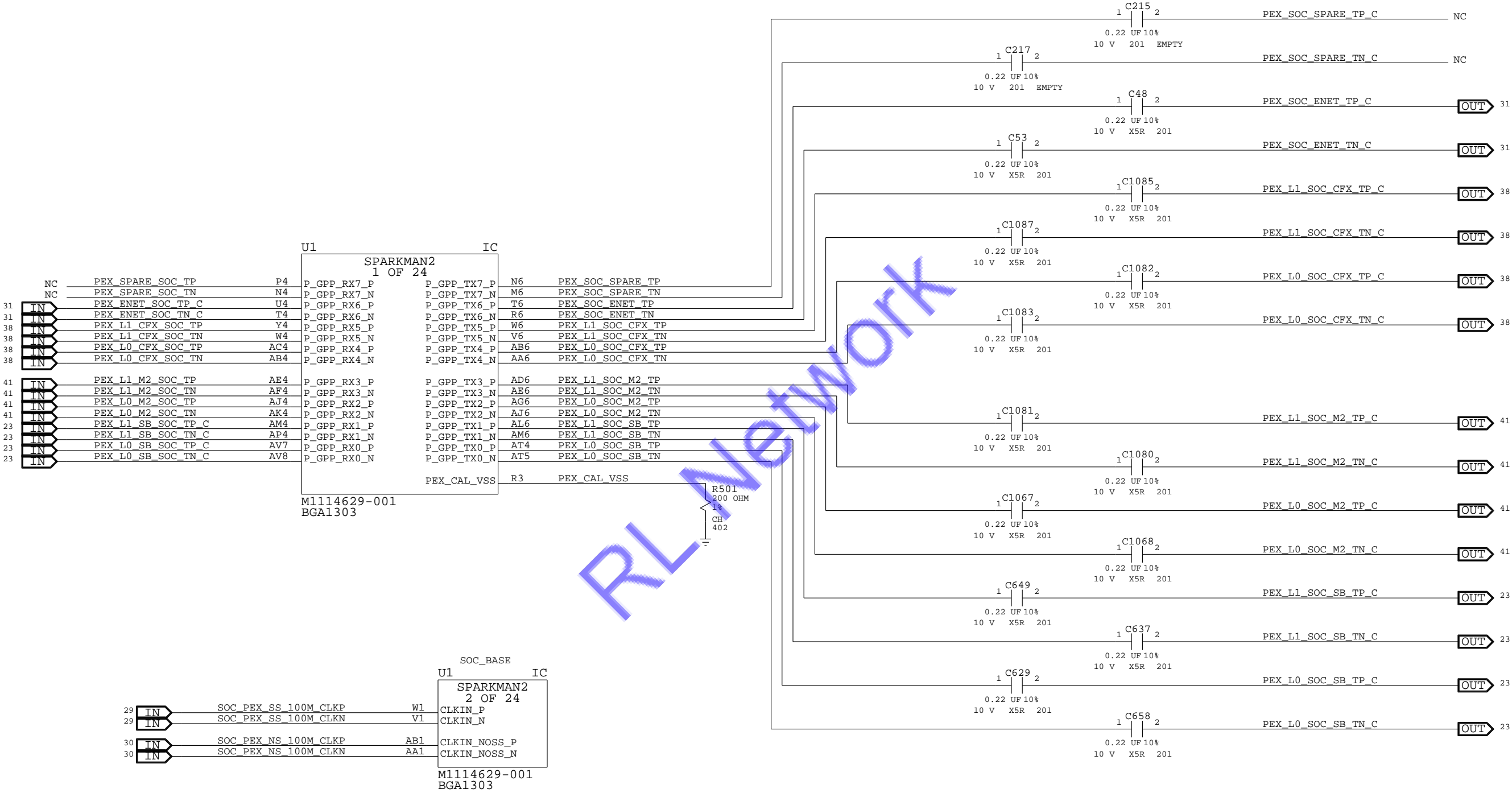


8		7		6		5		4		3		2		1	
D	SHEET	SHEET NAME		SHEET	SHEET NAME		STOCKTON FAB C REV 0.12								
	1	NONE		41	CONN: M.2										
	2	SOC: PCIE X, CLOCKS		42	CONN: ODD										
	3	SOC: VIDEO		43	CONN: FRONT PANEL, FAN, NEXUS										
	4	SOC POWER: MEMIO, CPUCORE, SOC		44	CONN: POWER										
	5	SOC: POWER: GFXCORE, MEMPHY, MISC		45	VREGS: V_12P0_GATED										
	6	SOC: POWER: VSS		46	VREGS: INPUT DECOUPLING										
	7	SOC: POWER: VSS		47	VREGS: V_CPUCORE, V_GFXCORE CONTROLLER										
C	8	SOC: DEBUG, SB SIGNALS, V_BAT, VOLTAGE SENSE		48	VREGS: V_GFXCORE OUTPUT PHASE 1 & 2										
	9	SOC: V_GFXCORE DECOUPLING		49	VREGS: V_GFXCORE OUTPUT PHASE 3 & 4										
	10	SOC: V_SOC DECOUPLING		50	VREGS: V_CPUCORE OUTPUT										
	11	SOC: V_MEMIO/V_MEMPHY DECOUPLING		51	VREGS: V_MEMIO, V_MEMPHY, V_SOC CONTROLLER										
	12	SOC: V_CPUCORE DECOUPLING		52	VREGS: V_MEMIO, V_MEMPHY, V_SOC SENSE										
	13	SOC & Memory: CHA/PHY0		53	VREGS: V_MEMIO AND V_MEMPHY OUTPUT										
	14	MEMORY: PWR/VSS & DECAP, A		54	VREGS: V_SOC OUTPUT										
	15	SOC & Memory: CHB/PHY1		55	VREGS: V_5P0										
B	16	MEMORY: PWR/VSS & DECAP, B		56	VREGS: V_SOC1P8, V_DRAM1P8										
	17	SOC & Memory: CHC/PHY2		57	VREGS: V_SOCPHY, V_FUSE										
	18	MEMORY: PWR/VSS & DECAP, C		58	VREGS: V_SB1P8, V_SB1P1										
	19	SOC & Memory: CHD/PHY3		59	VREGS: V_3P3STBY										
	20	MEMORY: PWR/VSS & DECAP, D		60	VREGS: V_3P3_GATED, V_3P3_CFX										
	21	SB: SMC		61	VREGS: V_1P1STBY, V_1P8STBY										
	22	SB: USB		62	I2C										
	23	SB: PCIE X, SATA, VIDEO		63	DEBUG: MARGIN V_SOCPHY, V_SOC1P8, V_DRAM1P8										
A	24	SB: SMM UART, SPI, JTAG, GPIO		64	DEBUG: MONITOR V_SOC1P8, V_SOCPHY, V_12P0, V_DRAM1P8										
	25	SB: POWER (VSS)		65	DEBUG: MONITOR M.2. CFEXPRESS										
	26	SB: POWER		66	DEBUG: FACET HEADER										
	27	SB: DECOUPLING		67	DEBUG: FTDI BRIDGE										
	28	SB: CLOCKS, STRAPPING, POR		68	DEBUG: FTDI BUFF, USB, PWR										
	29	CLOCK: PCIE 100MHZ SS		69	DEBUG: SWITCHES, LEDS										
	30	CLOCK: PCIE 100MHZ NS		70	DEBUG: HDT										
	31	ETHERNET CONTROLLER		71	DEBUG: VR HEADERS, TEST POINTS, CONNECTORS										
	32	SB: EMMC (LEGACY)		72	LABELS AND MOUNTING										
	33	MEMORY: SPI FLASH SOC		73	BOM DEFINITIONS										
	34	MEMORY: SPI FLASH		74	STOCKTON_NEXUS										
	35	HDMI: VIDEO OUT		75	B2B CONN AND LABELS										
	36	HDMI: LOAD SWITCHES		76	NEXUS LED AND POWER SWITCH										
	37	AUDIO: PREMIUM AND RETAIL													
	38	CONN: RJ45, SPDIF, CFEXPRESS													
	39	CONN: USB (FRONT & REAR)													
	40	CONN: WIFI													
RULES: (APPLIED WHEN POSSIBLE) 1. MSB TO LSB IS TOP TO BOTTOM 2. WHEN POSSIBLE: INPUTS ON LEFT, OUTPUTS ON RIGHT 3. ORDER OF PAGES=CHIP INTERFACES, TERMINATION, POWER, DECOUPLING 4. AVOID USING OFF PAGE CONNECTORS FOR ON PAGE CONNECTIONS 5. LANED SIGNALS ARE GROUPED ON SYMBOLS 6. TRANSMITTER NAME USED AS PREFIX WITH RX AND TX CONNECTIONS 7. SUFFIX V IS USED FOR VOLTAGE RAIL SIGNAL NAMES 8. SUFFIX _DP AND _DN ARE USED FOR DIFFERENTIAL PAIRS 9. UNNAMED NETS ARE NAMED WITH /2 TEXT SIZE 10.SUFFIX _N FOR ACTIVE LOW OR N JUNCTION 12.SUFFIX _P FOR P JUNCTION 13.SUFFIX _EN FOR ENABLE 14.'CLK' FOR CLOCKS, 'RST' FOR RESETS 15.PWRGD FOR POWER GOOD 16.REV AND FAB ARE SET USING CUSTOM VARIABLES TOOLS>OPTIONS>VARIABLES															
DRAWING Tue Jun 25 13:39:30 2019															
MICROSOFT CONFIDENTIAL		PROJECT NAME Stockton		PAGE 1/76		CSA PAGE 1/76		FAB C		VER 0.12					
8		7		6		5		4		3		2		1	

SOC: PCIE X, CLOCKS



MXXXXXXX-001	MATL	REF DES	DESCR.	BOM PROPERTY
M1114629-001	IC	U1	PROCSR,SOC,SM,1304-BGA,SPARKMAN35	SOC_INCLUDE
M1114629-001	EMPTY	U1	PROCSR,SOC,SM,1304-BGA,SPARKMAN35	SOC_EMPTY

MICROSOFT CONFIDENTIAL	PROJECT NAME Stockton	PAGE 2/76	CSA PAGE 2/76	FAB C	VER 0.12
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8

7

6

5

4

3

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1

SOC: VIDEO

35

OUT

35

OUT

35

OUT

35

OUT

35

OUT

35

OUT

35

OUT

35

OUT

35

BT

35

BT

35

IN

TMDS\_TX\_DP2

TMDS\_TX\_DN2

TMDS\_TX\_DP1

TMDS\_TX\_DN1

TMDS\_TX\_DP0

TMDS\_TX\_DN0

TMDS\_TX\_CLKP

TMDS\_TX\_CLKN

SOC\_DDC\_CLK

SOC\_DDC\_DATA

DP0\_HPD

DP\_AUX\_CALR

T1

R1

N1

M1

J1

H1

E1

D1

A4

A5

K2

G2

DP0\_TX0\_P

DP0\_TX0\_N

DP0\_TX1\_P

DP0\_TX1\_N

DP0\_TX2\_P

DP0\_TX2\_N

DP0\_TX3\_P

DP0\_TX3\_N

DP0\_AUX\_P

DP0\_AUX\_N

3P3V\_DP0\_HPD

DP\_CAL\_ZVSS

U1

IC

SPARKMAN2

3 OF 24

M1114629-001

BGA1303

3P3V\_CIO\_PLUG\_DET

3P3V\_SLEEP\_S3\_N

3P3V\_FORCE\_PWR

HDMI\_EN\_PIN\_STRP

3P3V\_SPDIF\_OUT

3P3V\_SPDIF\_DETECT

AT1

AU2

AV3

P2

A8

B8

3P3V\_CIO\_PLUG\_DET

3P3V\_SLEEP\_S3\_N

3P3V\_FORCE\_PWR

HDMI\_EN\_PIN\_STRP

SPDIF\_OUT

SPDIF\_DETECT

NC

OUT

OUT

OUT

OUT

IN

51

51

38

38

V\_SOC1P8

R487

1 KOHM

1%

CH

201

R491

1 KOHM

1%

EMPTY

201

1

2

1

2

R557

200 OHM

1%

CH

402

1

2

RL Network

DVI PCB ROUTING ORDERING	DP PCB ROUTING ORDERING	PIN NAME
TMDS CLOCK -	DP LANE 3 -	DP0_TX3_N
TMDS CLOCK +	DP LANE 3 +	DP0_TX3_P
TMDS DATA0 -	DP LANE 2 -	DP0_TX2_N
TMDS DATA0 +	DP LANE 2 +	DP0_TX2_P
TMDS DATA1 -	DP LANE 1 -	DP0_TX1_N
TMDS DATA1 +	DP LANE 1 +	DP0_TX1_P
TMDS DATA2 -	DP LANE 0 -	DP0_TX0_N
TMDS DATA2 +	DP LANE 0 +	DP0_TX0_P

MICROSOFT  
CONFIDENTIAL

PROJECT NAME  
Stockton

PAGE  
3/76

CSA  
PAGE  
3/76

FAB  
C

VER  
0.12

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1

A

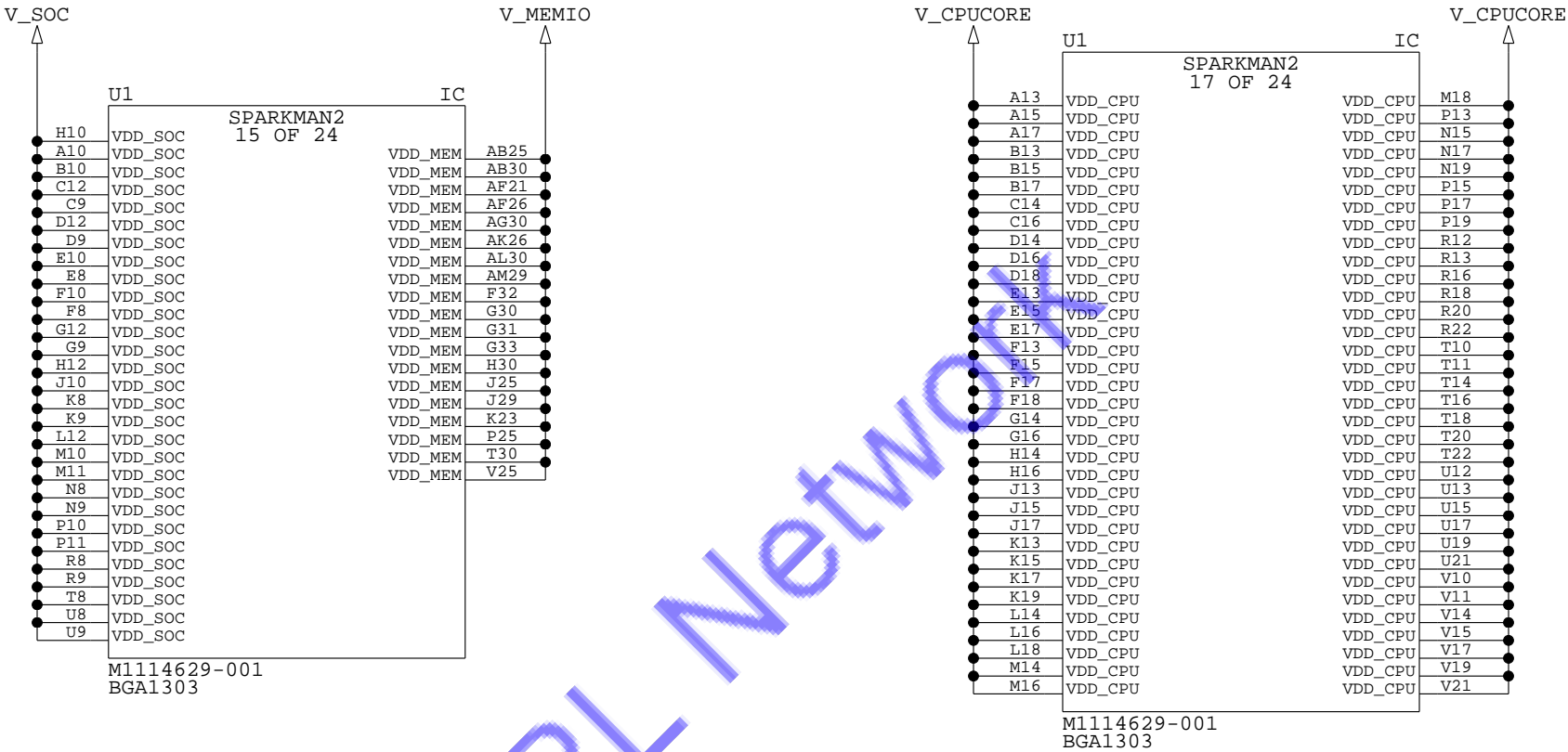
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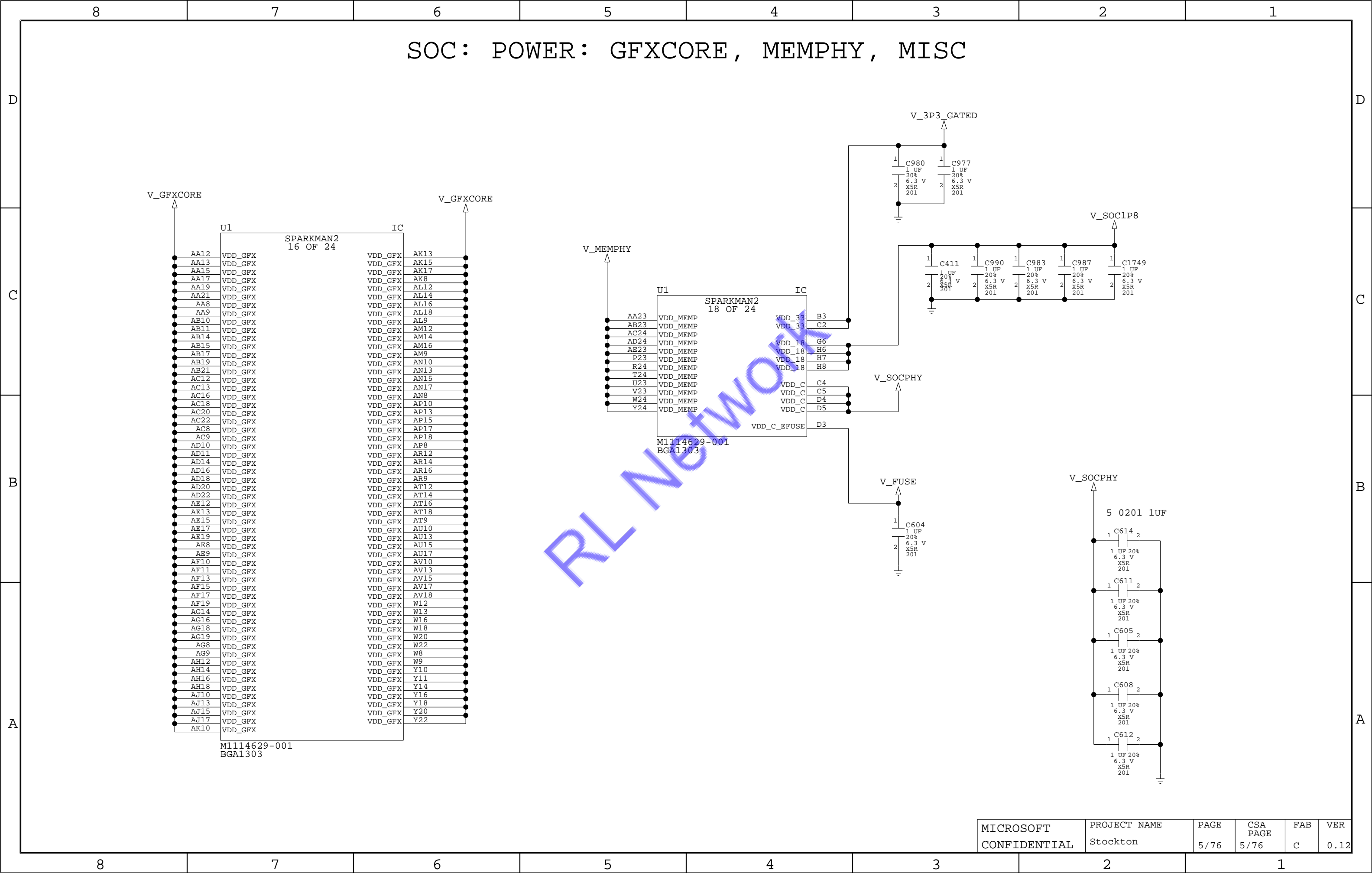
C

D

DVI PCB ROUTING ORDERING	DP PCB ROUTING ORDERING	PIN NAME
TMDS CLOCK -	DP LANE 3 -	DP0_TX3_N
TMDS CLOCK +	DP LANE 3 +	DP0_TX3_P
TMDS DATA0 -	DP LANE 2 -	DP0_TX2_N
TMDS DATA0 +	DP LANE 2 +	DP0_TX2_P
TMDS DATA1 -	DP LANE 1 -	DP0_TX1_N
TMDS DATA1 +	DP LANE 1 +	DP0_TX1_P
TMDS DATA2 -	DP LANE 0 -	DP0_TX0_N
TMDS DATA2 +	DP LANE 0 +	DP0_TX0_P

SOC POWER: MEMIO, CPUCORE, SOC





MICROSOFT  
CONFIDENTIAL

PROJECT NAME  
Stockton

PAGE  
5/76

CSA  
PAGE  
5/76

FAB  
C

VER  
0.12



8 7 6 5 4 3 2 1

SOC: POWER: VSS

D

C

B

A

8 7 6 5 4 3 2 1

U1 IC  
SPARKMAN2  
23 OF 24

U1 IC  
SPARKMAN2  
24 OF 24

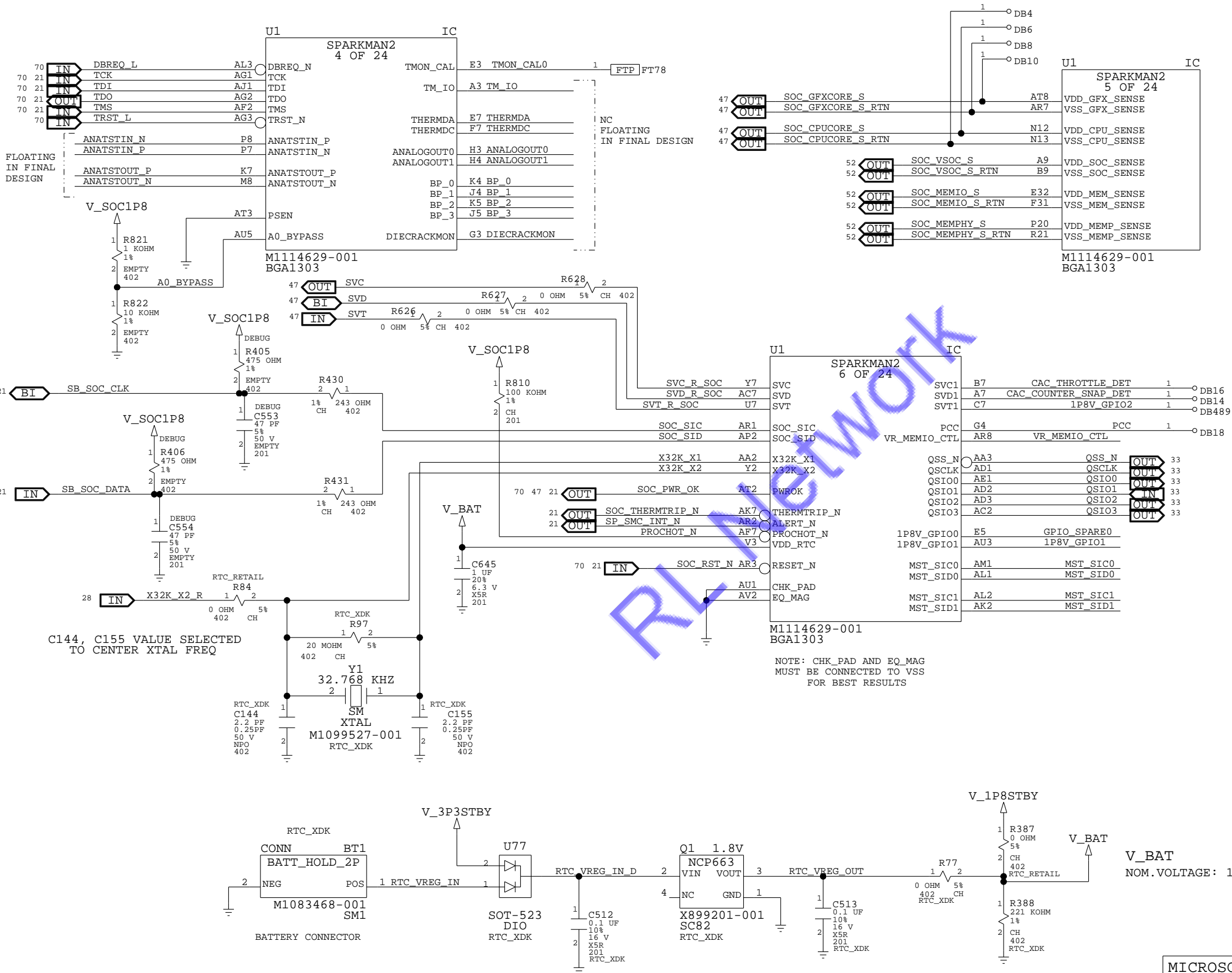
M1114629-001  
BGA1303

M1114629-001  
BGA1303

MICROSOFT	PROJECT NAME	PAGE	CSA	FAB	VER
CONFIDENTIAL	Stockton	7/76	PAGE 7/76	C	0.12



SOC: DEBUG, SB SIGNALS, V\_BAT, VOLTAGE SENSE

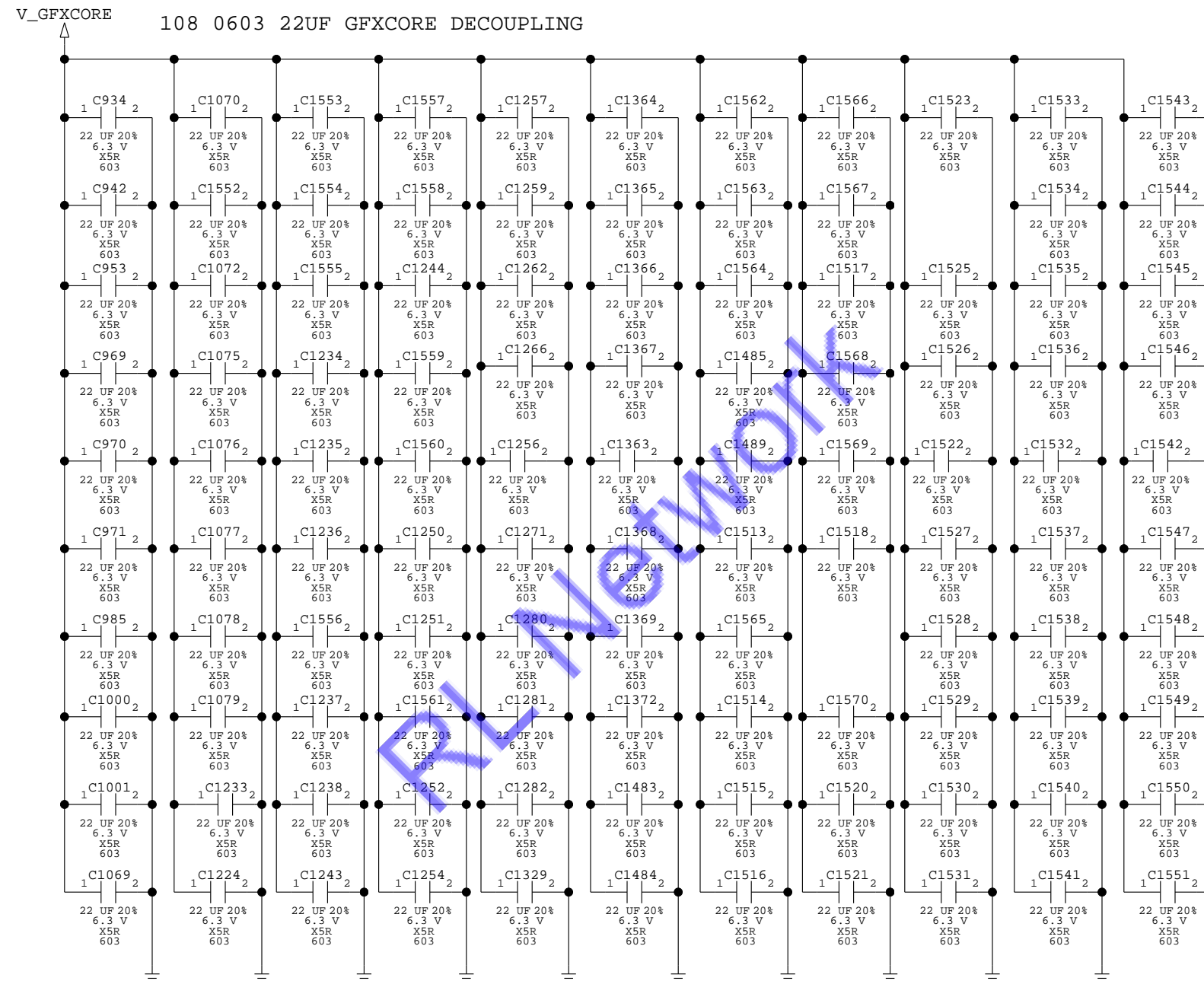


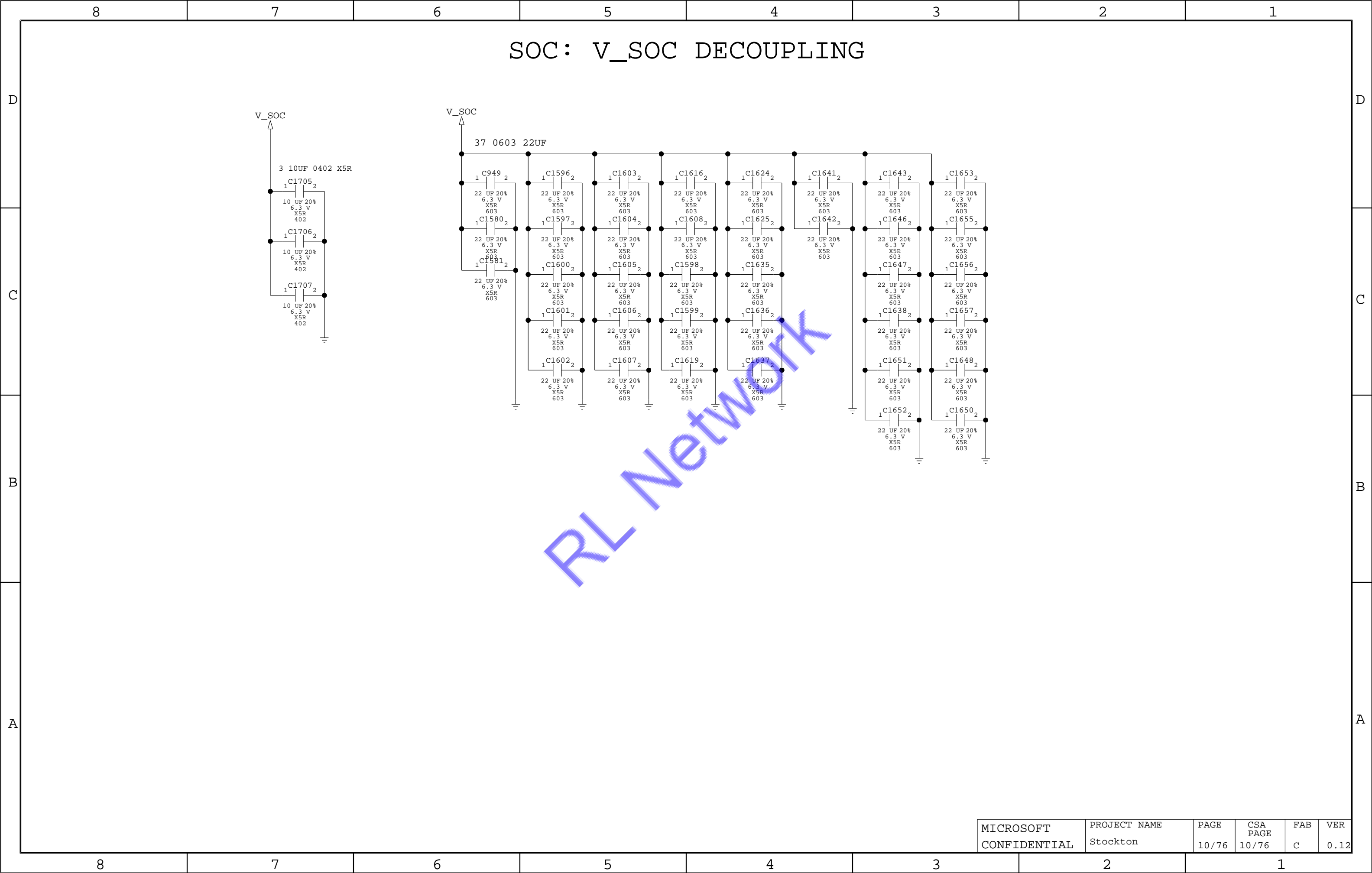
STUFF R388 IF SOC IS NOT STUFFED

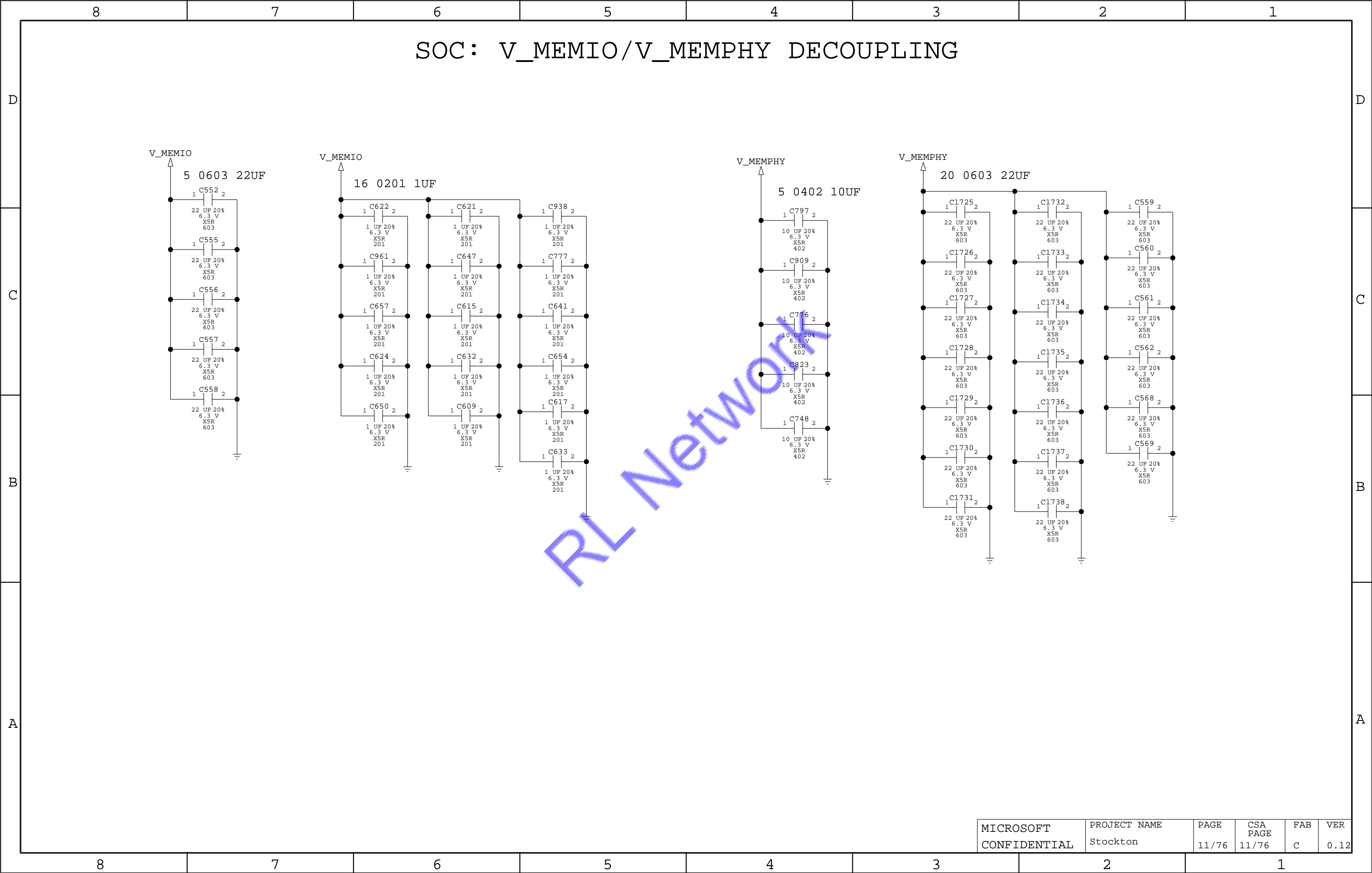
MICROSOFT	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
CONFIDENTIAL	Stockton	8/76	8/76	C	0.12



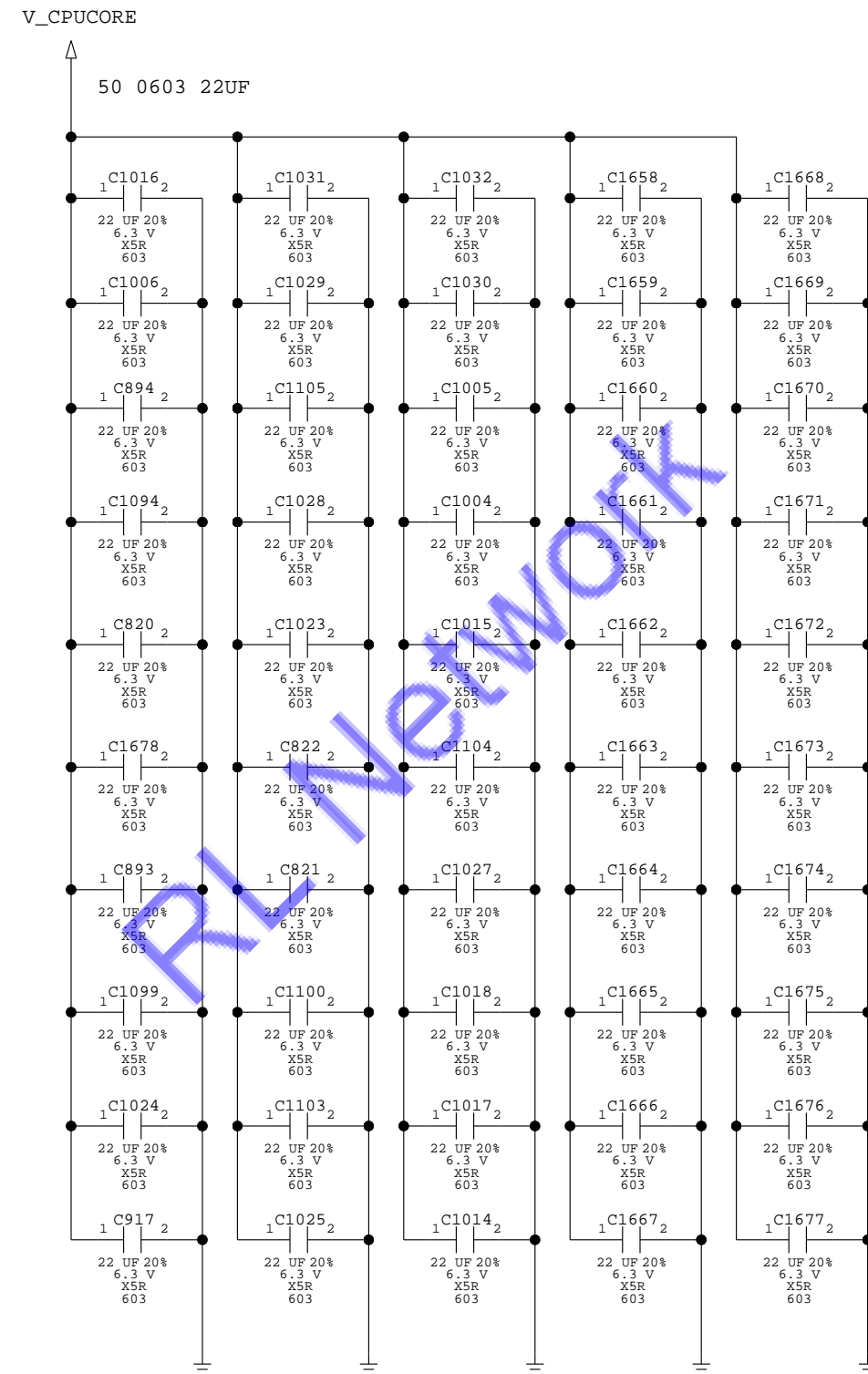
## SOC: V\_GFXCORE DECOUPLING







## SOC: V\_CPUCORE DECOUPLING

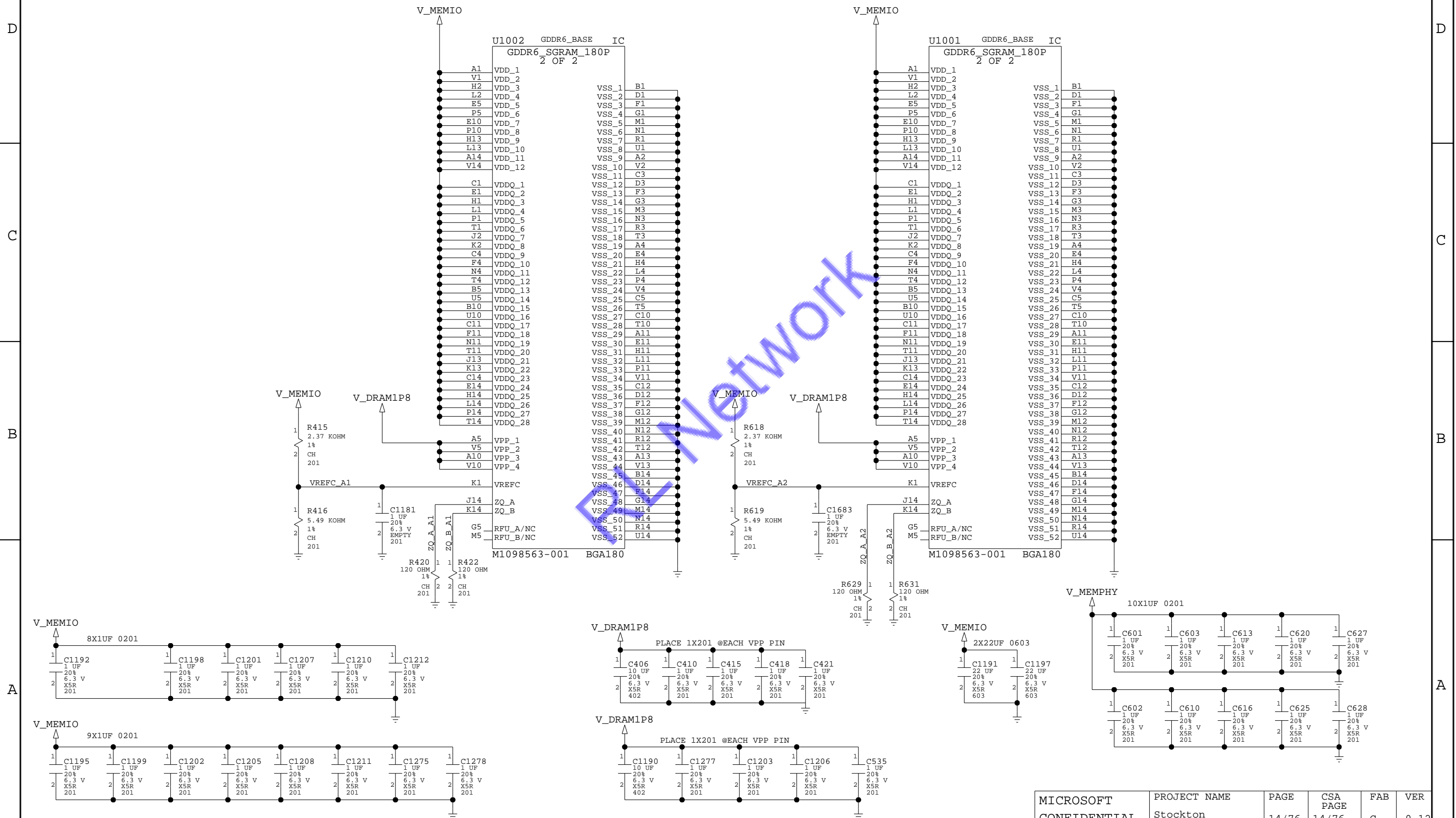


8	7	6	5	4	3	2	1
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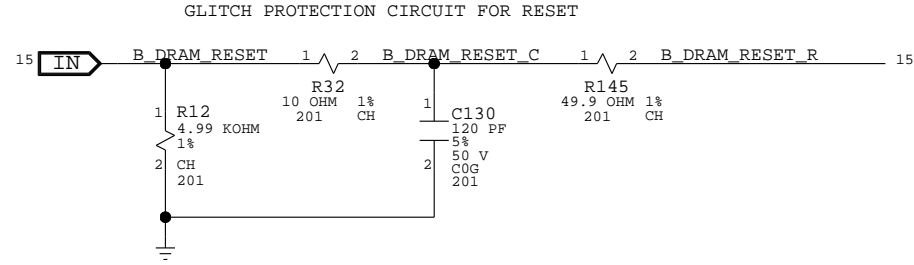
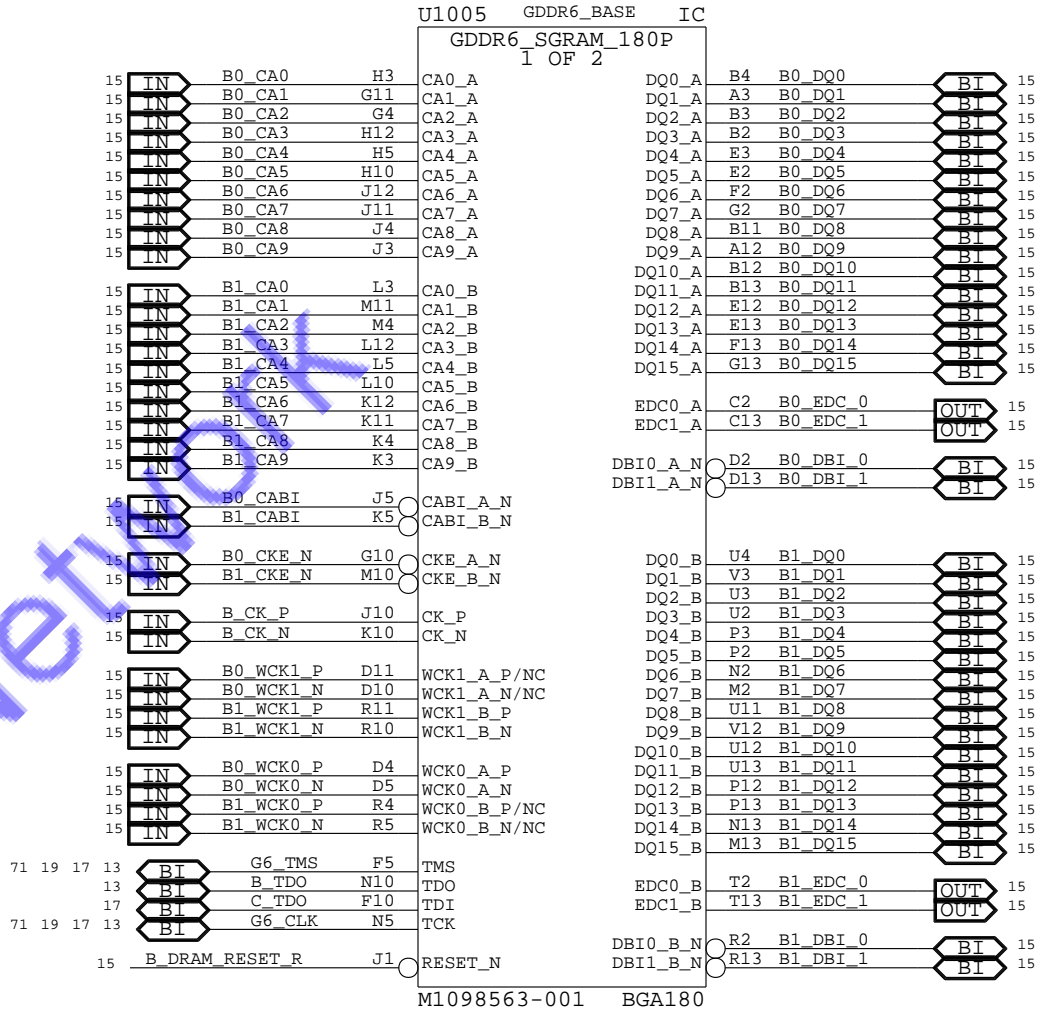
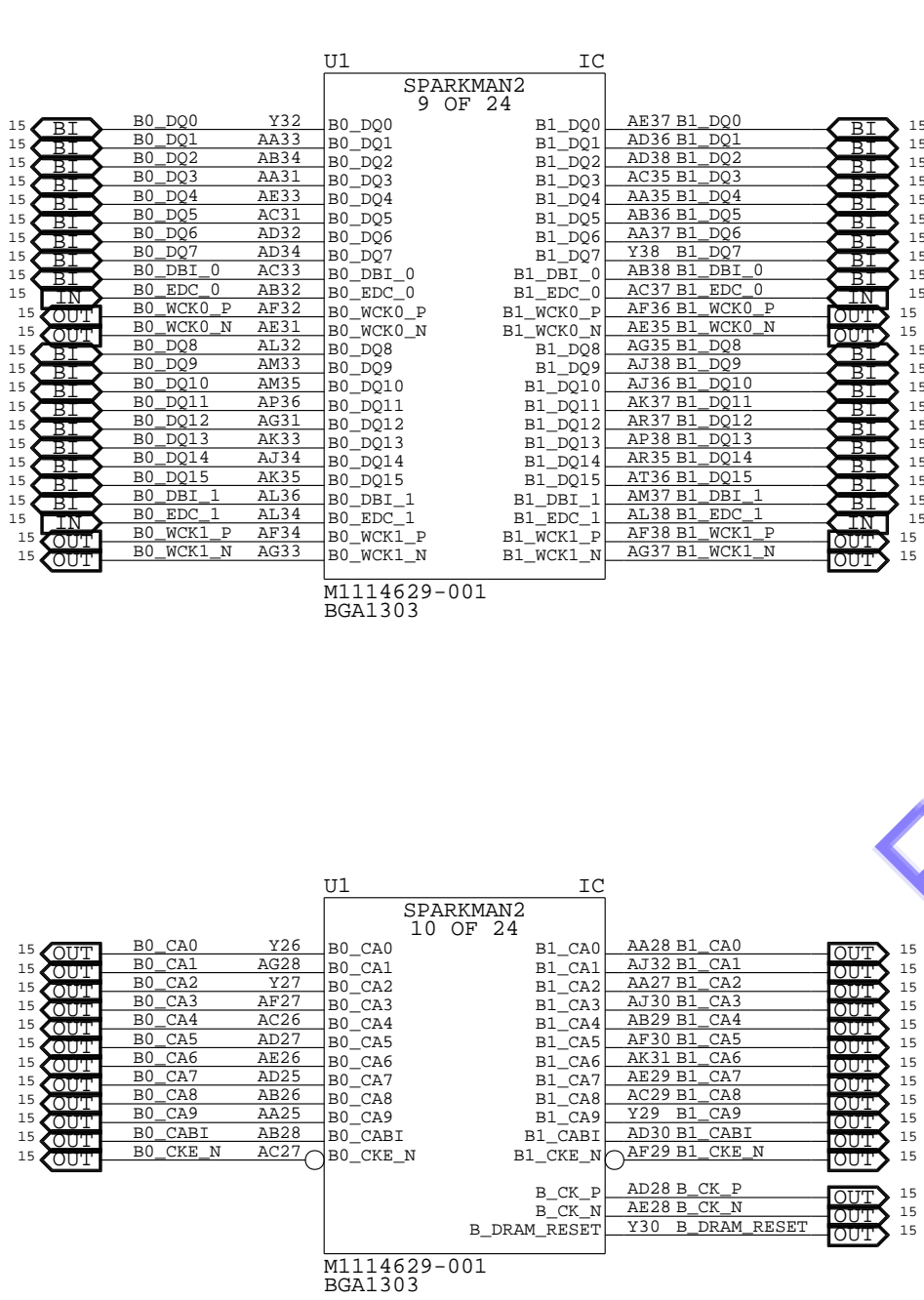
A

8	7	6	5	4	3	2	1
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MEMORY: PWR/VSS & DECAP, A

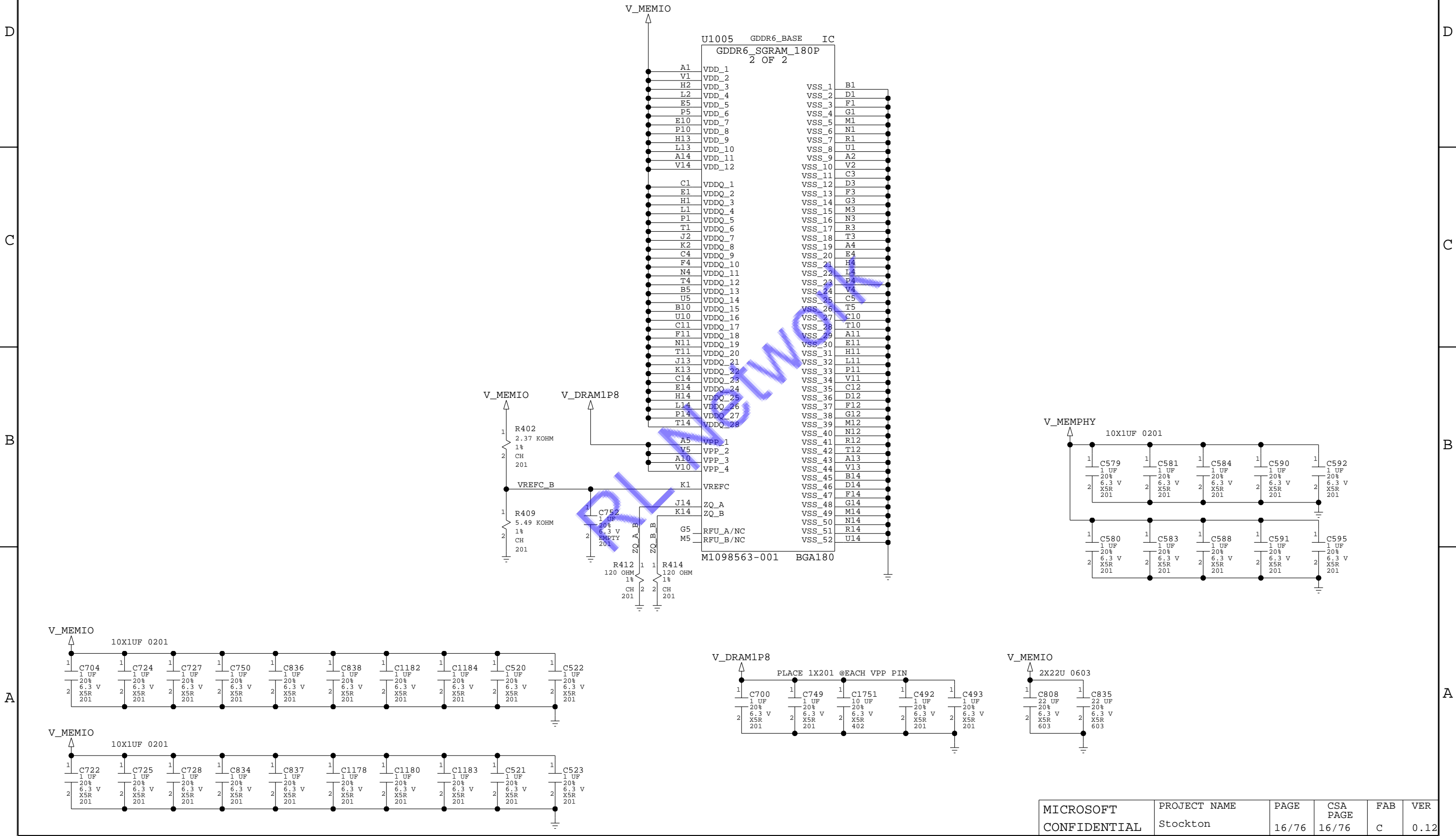


SOC & Memory: CHB/PHY1

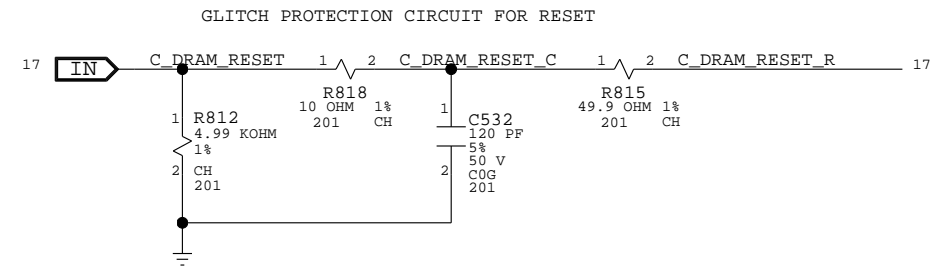
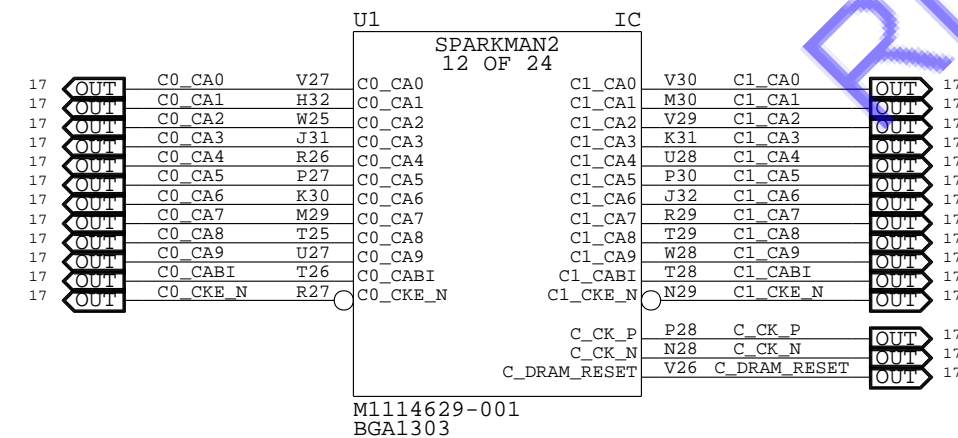




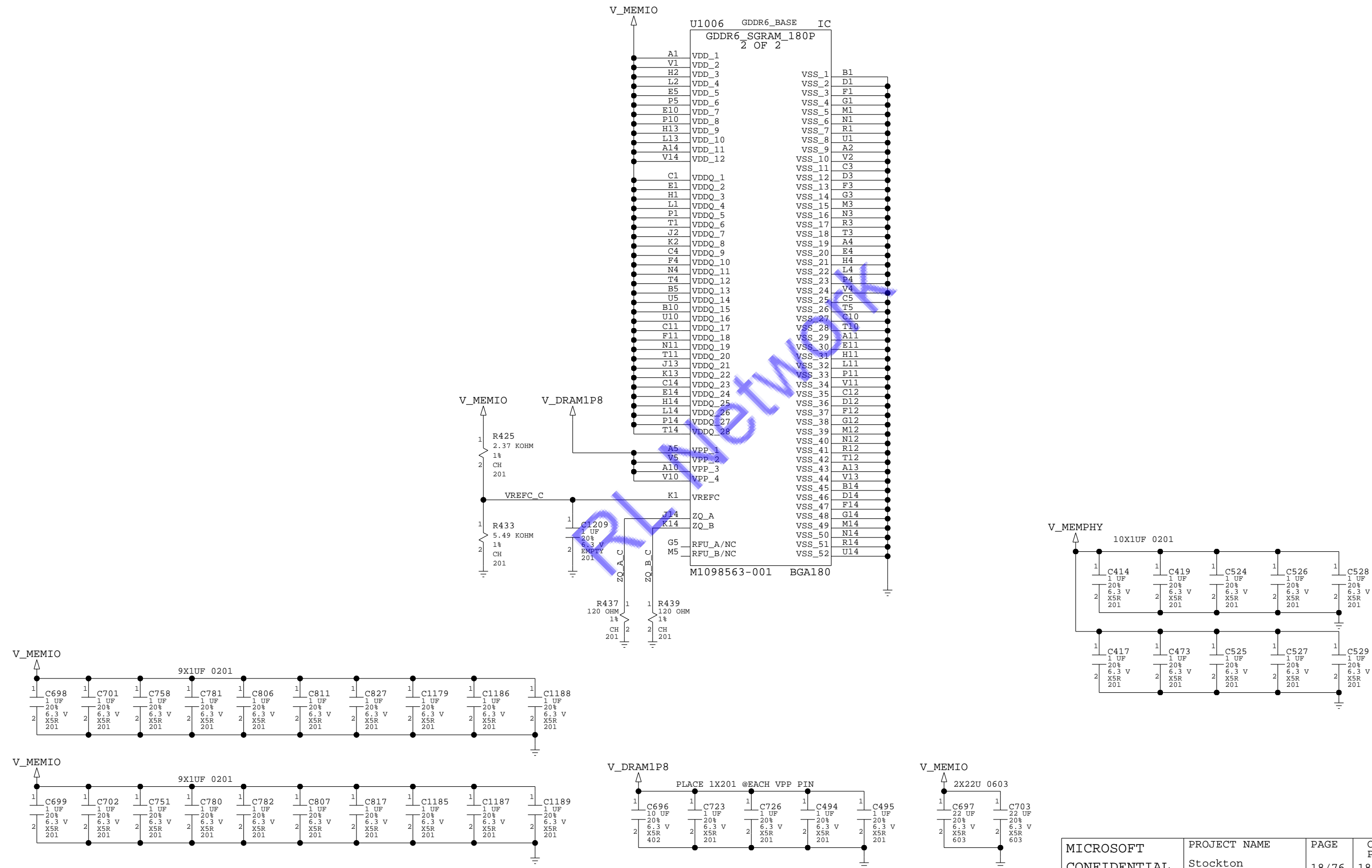
MEMORY: PWR/VSS & DECAP, B



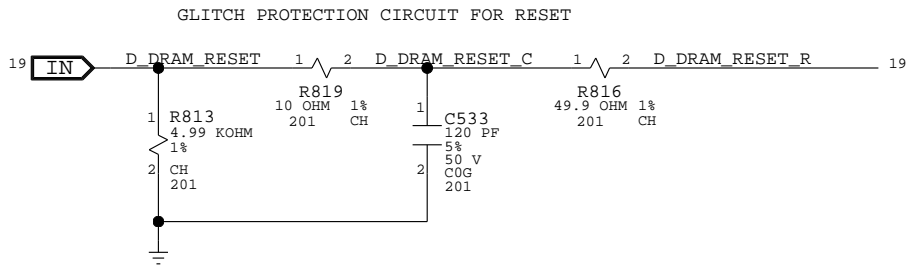
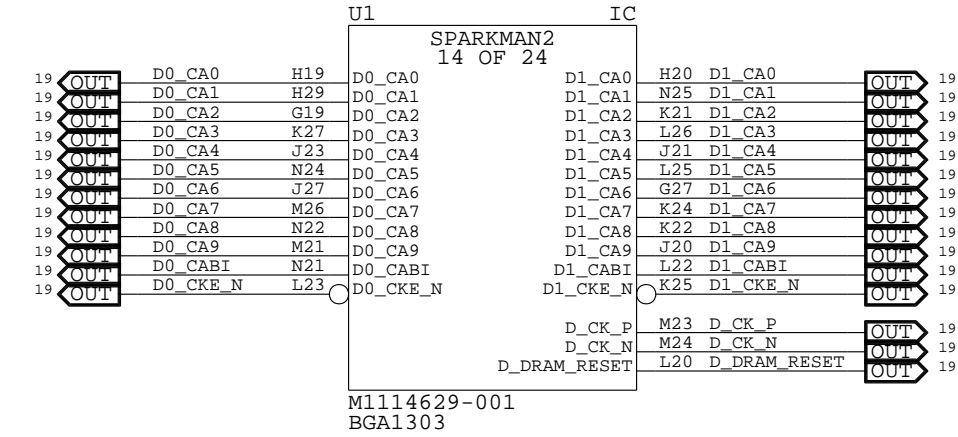
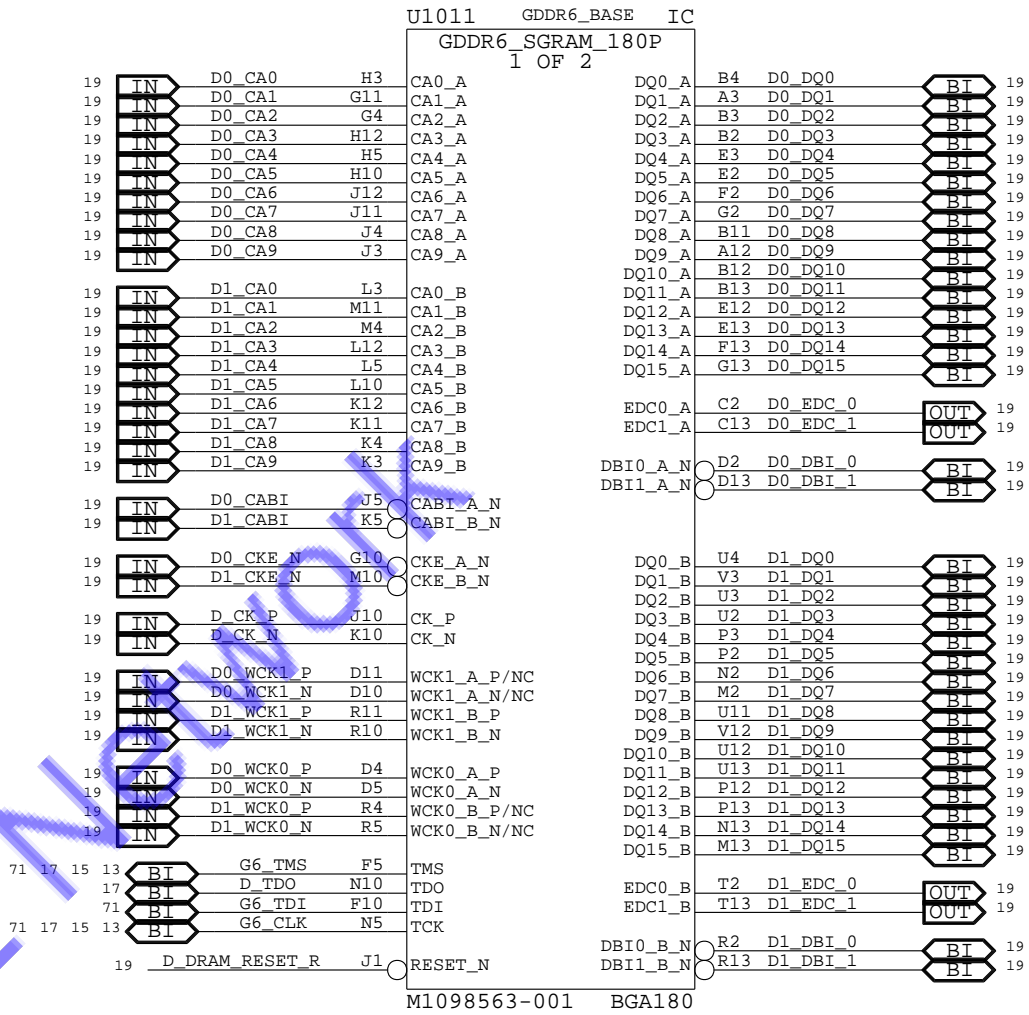
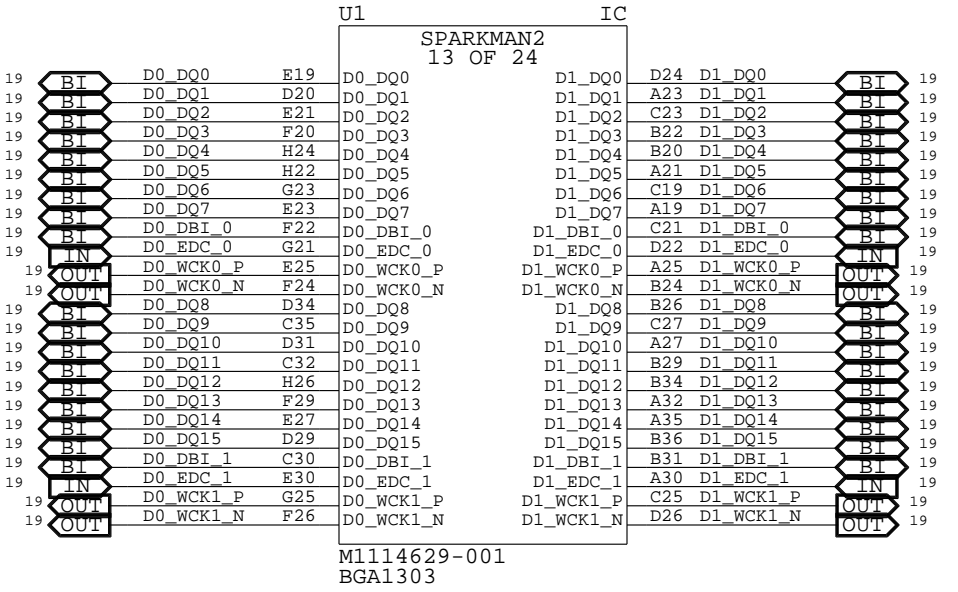
1	B1	17
2	B1	17
3	B1	17
4	B1	17
5	B1	17
1	B1	17
1	B1	17
1	IN	17
1	OUT	17
1	OUT	17

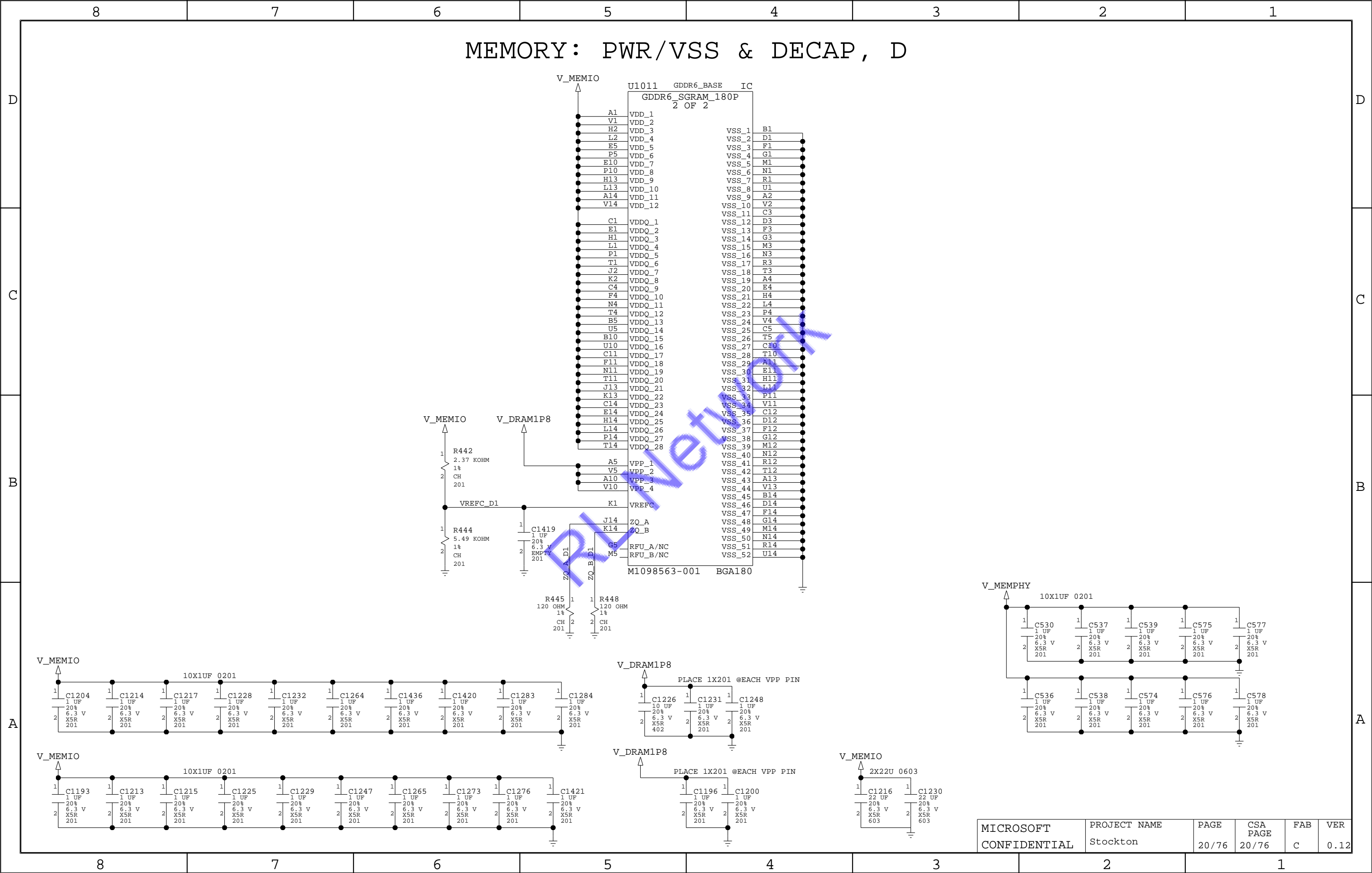


MEMORY: PWR/VSS & DECAP, C

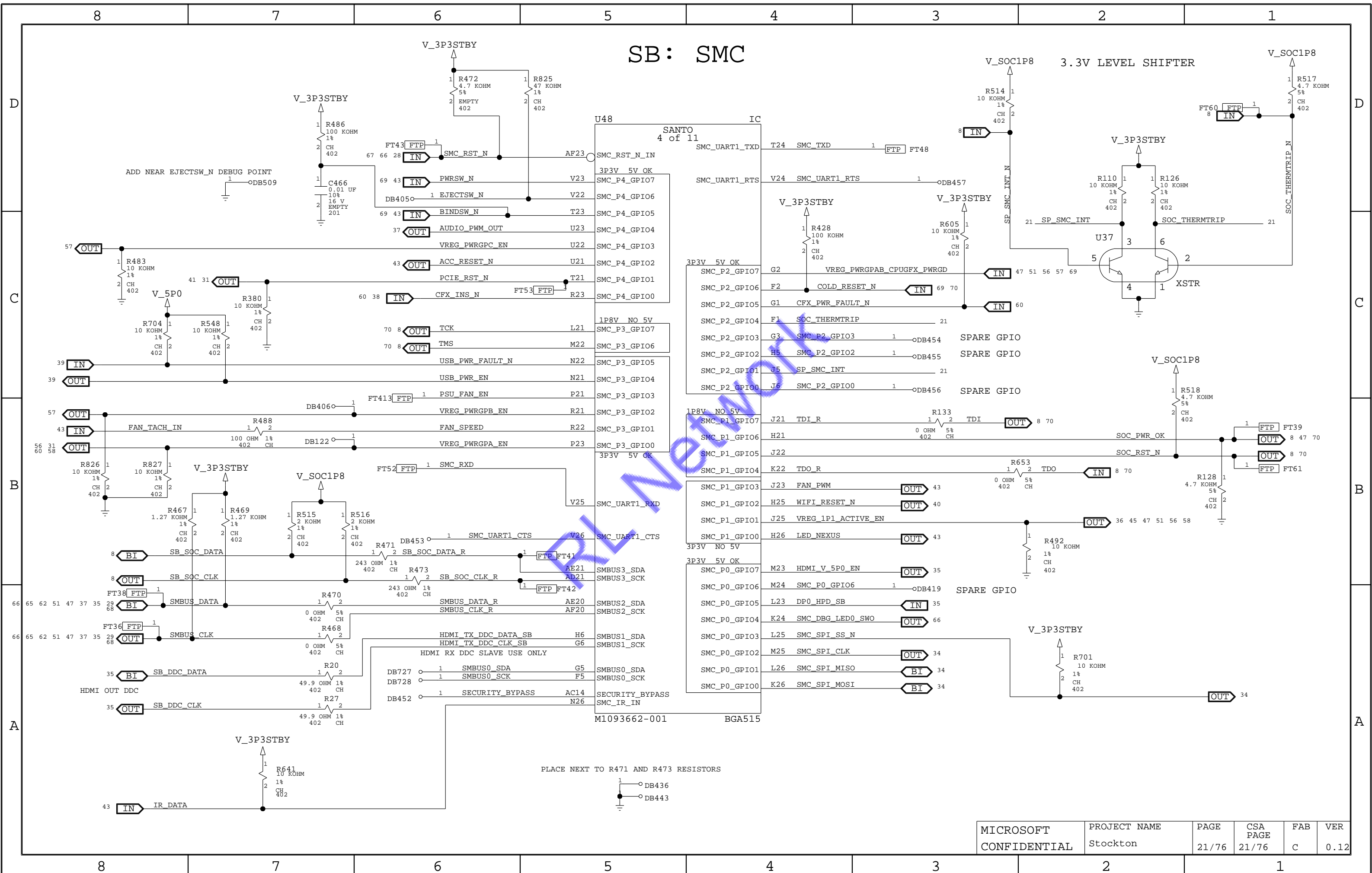


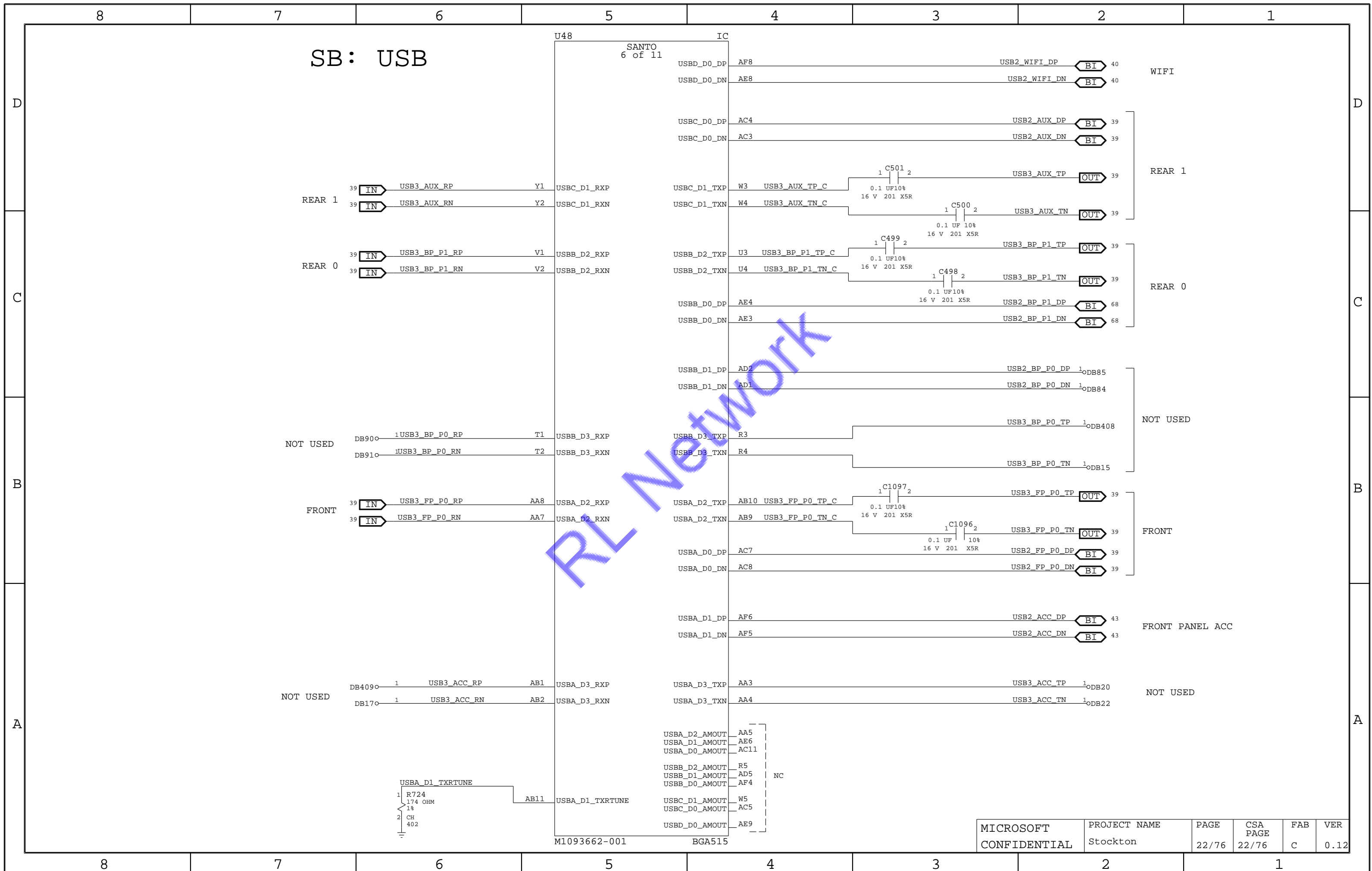
SOC & Memory: CHD/PHY3





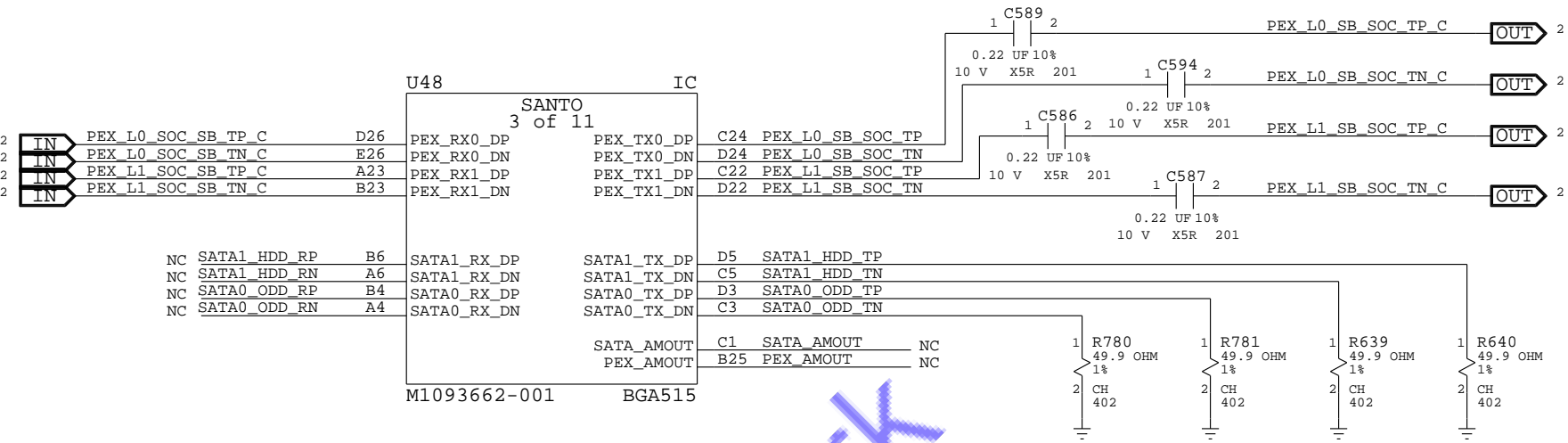




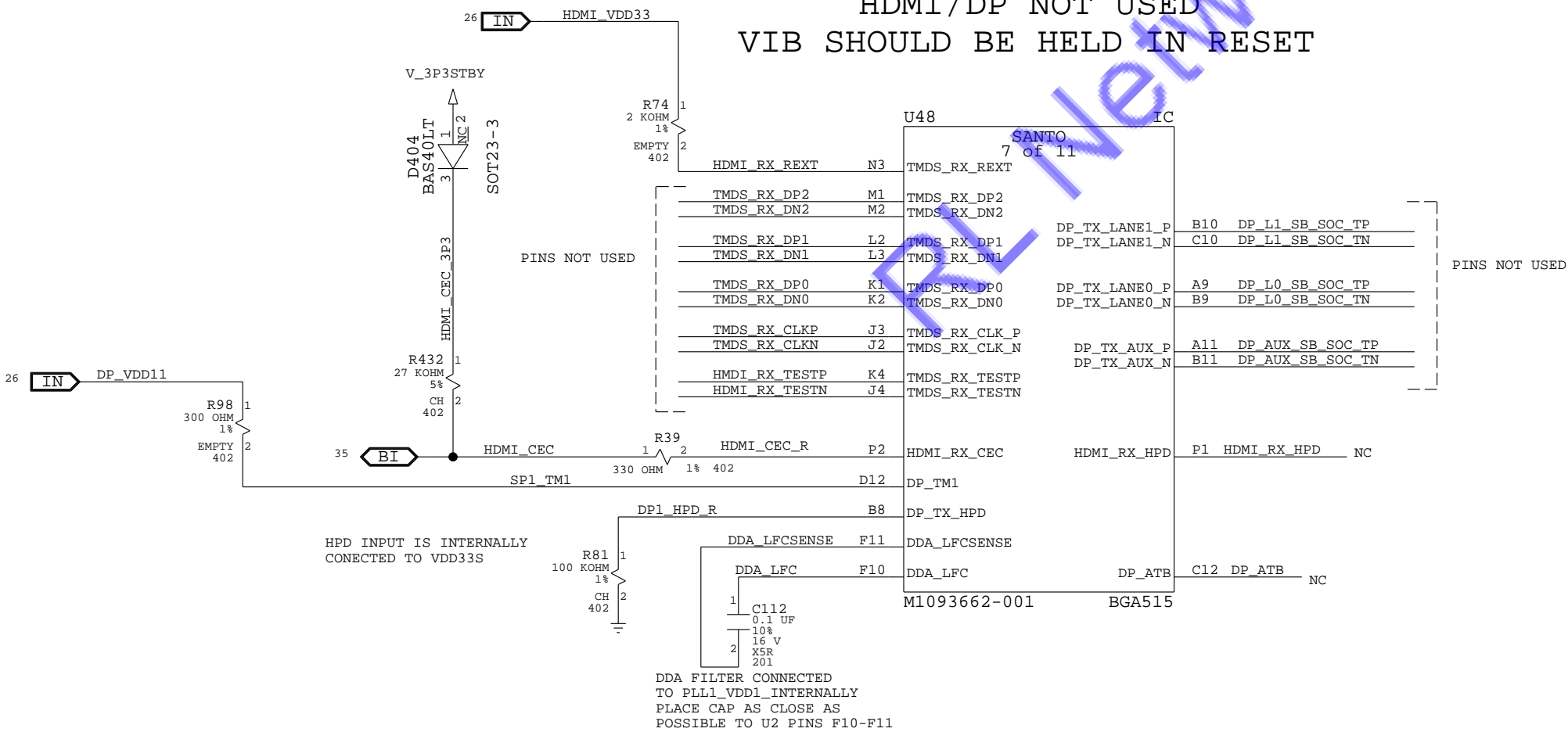




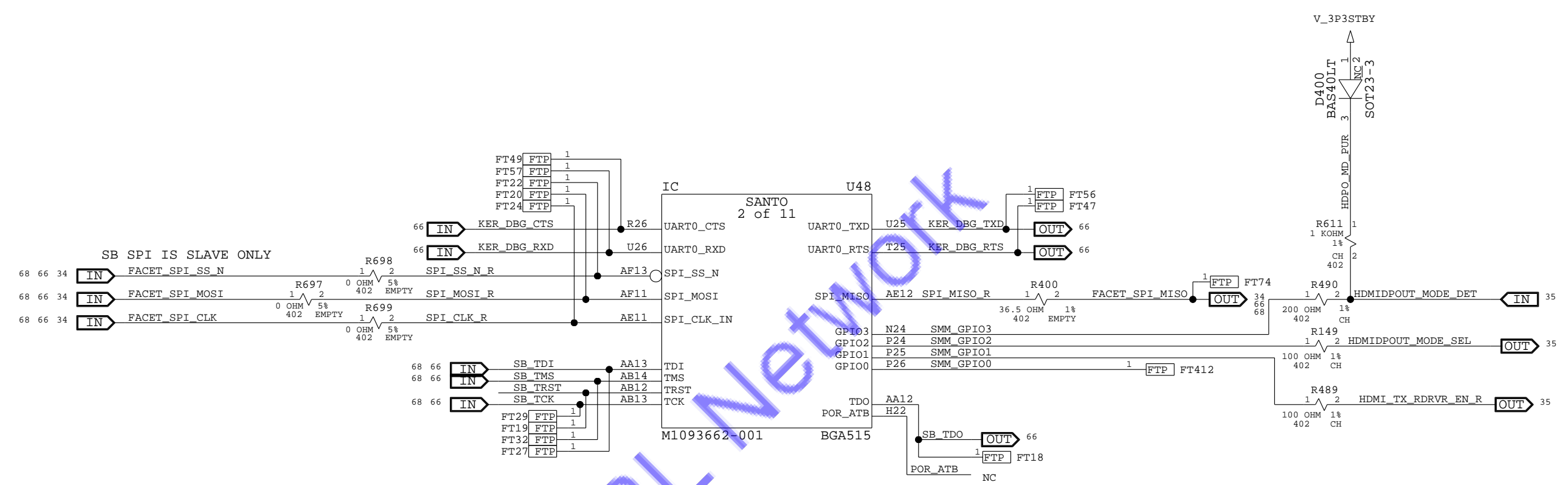
SB: PCIE, SATA, VIDEO

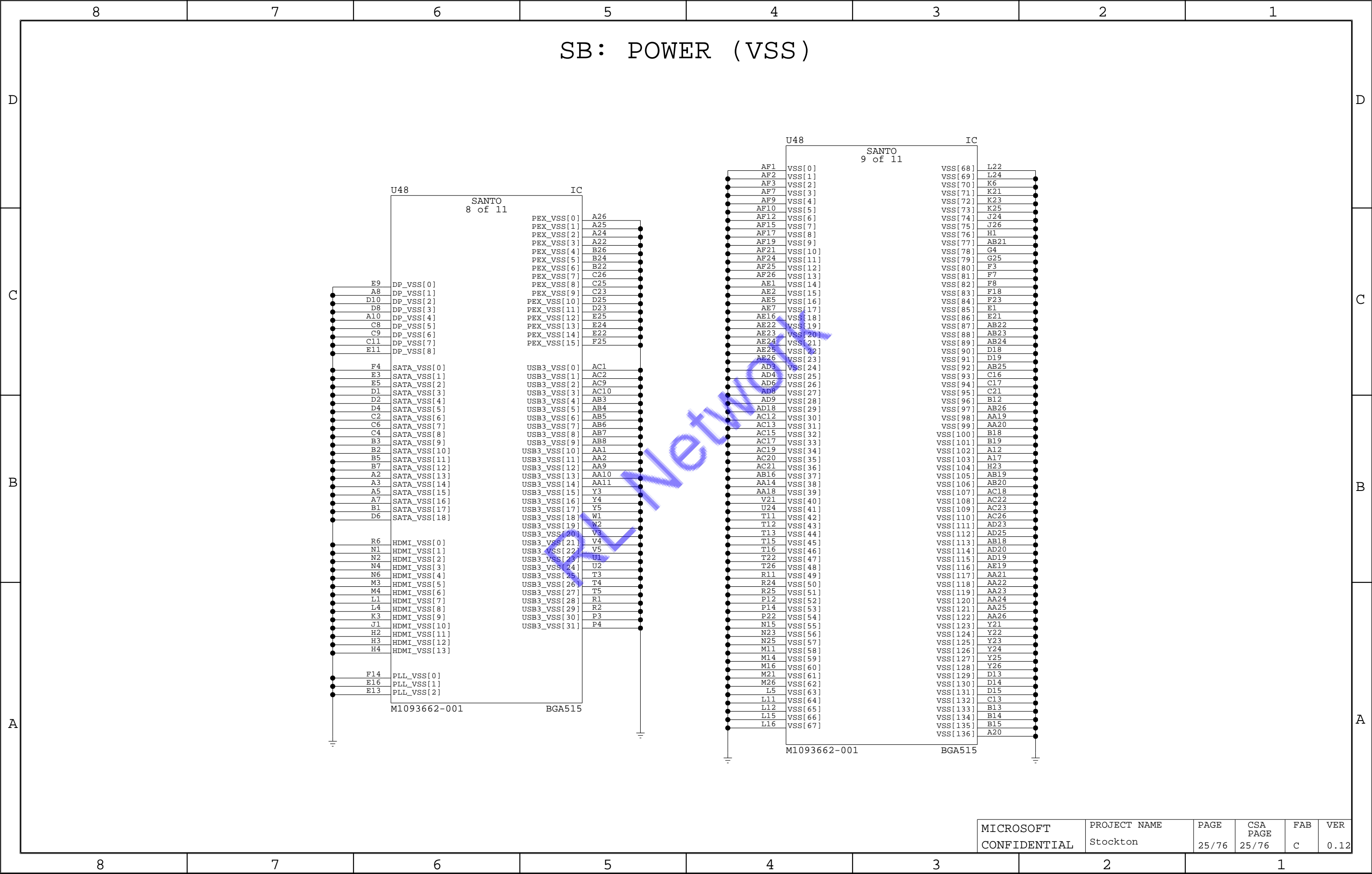


HDMI/DP NOT USED  
VIB SHOULD BE HELD IN RESET



SB: SMM UART, SPI, JTAG, GPIO





SB: POWER

POWER REMOVED FROM AUX AND HDMI

IC

OUT 23

V\_3P3

V\_SB1P1

V\_SB1P1

V\_SB1P1

V\_SB1P1

V\_SB1P1

V\_SB1P1

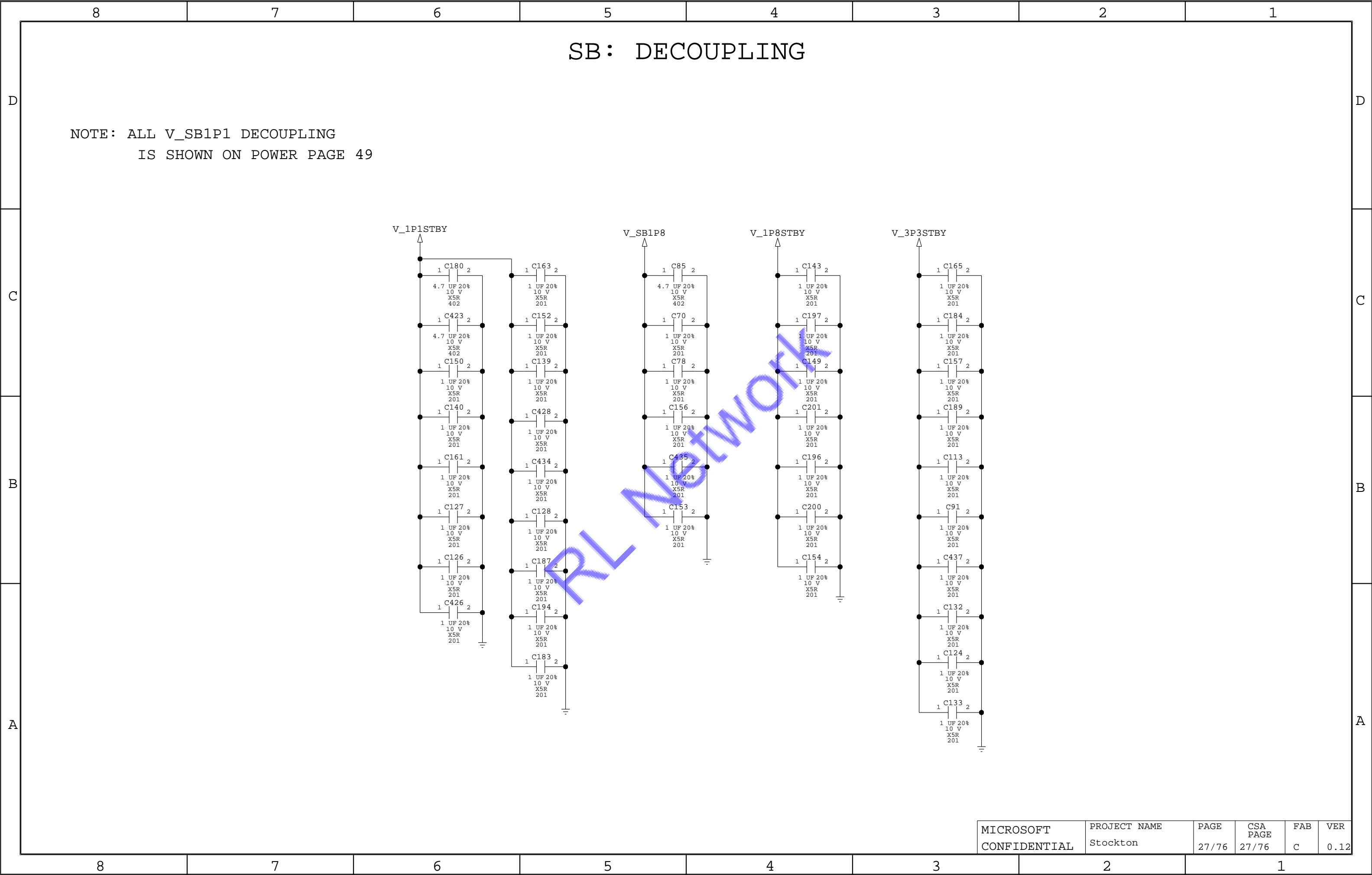
POWER REMOVED FROM DP

IC

OUT 23

V\_SB1P1

MICROSOFT CONFIDENTIAL	PROJECT NAME Stockton	PAGE 26/76	CSA PAGE 26/76	FAB C	VER 0.12
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MICROSOFT  
CONFIDENTIAL

PROJECT NAME  
Stockton

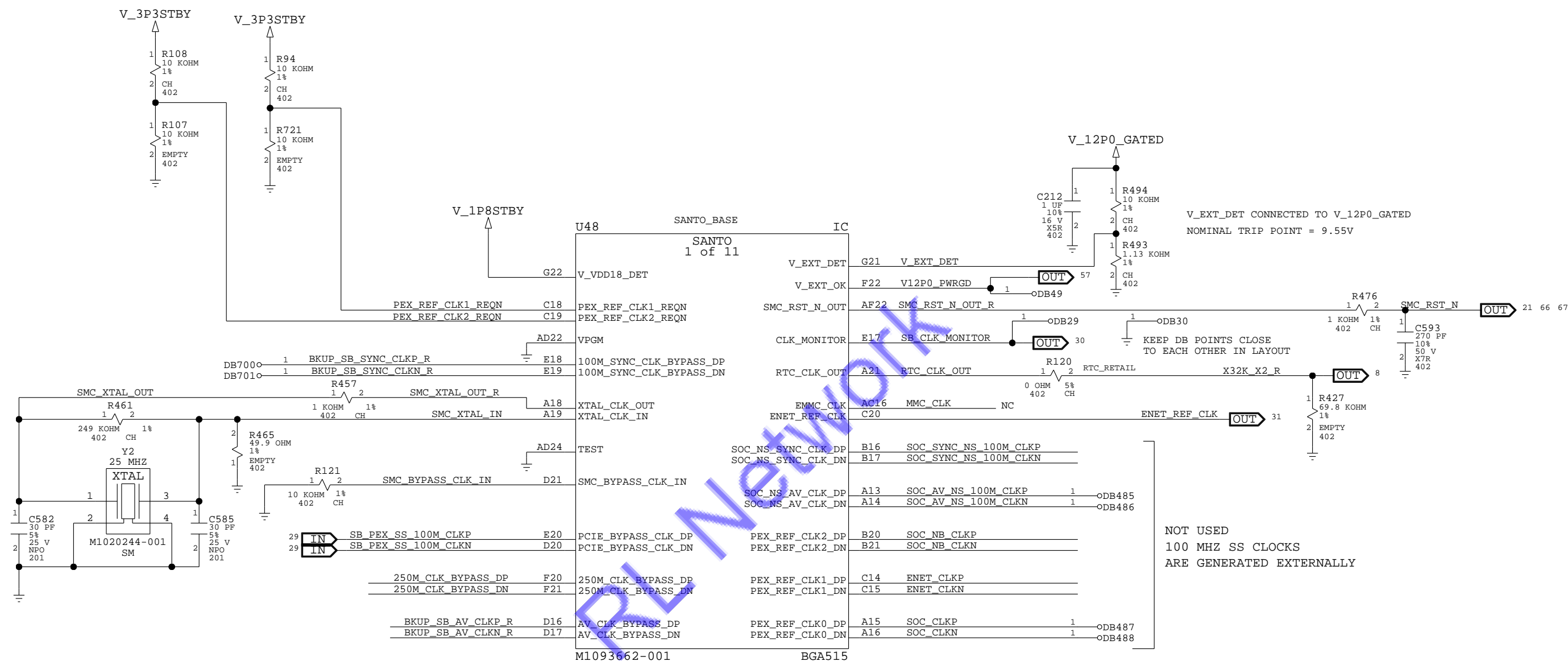
PAGE  
27/76

CSA  
PAGE  
27/76

FAB  
C

VER  
0.12

SB: CLOCKS, STRAPPING, POR



MXXXXXXX-001	MATL	REF DES	DESCR.	BOM PROPERTY
M1093668-001	IC	U48	IC,SANTO SB,BGA515	SANTO_RETAIL
M1093662-001	IC	U48	IC,SANTO SB,BGA515	SANTO_DEV
M1093668-001	EMPTY	U48	IC,SANTO SB,BGA515	SANTO_EMPTY

MICROSOFT CONFIDENTIAL	PROJECT NAME Stockton	PAGE 28/76	CSA PAGE 28/76	FAB C	VER 0.12
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CLOCK: PCIE 100MHZ SS

9FGL0651 SMBUS ADDRESS  
1101 010 R/W HEX  
WRITE 1101 010 0 0XD4  
READ 1101 010 1 0XD5

POWER SUBJECT TO REVIEW

85 OHM DIFF OUTPUTS

R166 = 1K TO ACCOUNT FOR ~60KOHM COMBINED INPUT IMPEDANCE OF CLOCK GENS

MICROSOFT	PROJECT NAME	PAGE	CSA	FAB	VER
CONFIDENTIAL	Stockton	29/76	29/76	C	0.12

I2C BUFFER PREVENTS LEAKAGE PATH FROM SMBUS PULLUPS TO V\_3P3\_GATED THROUGH CLOCK GENERATORS

EN: 450K INTERNAL PU TO VCCA  
V\_3P3\_SS\_CLK HAS 10K PD TO GND

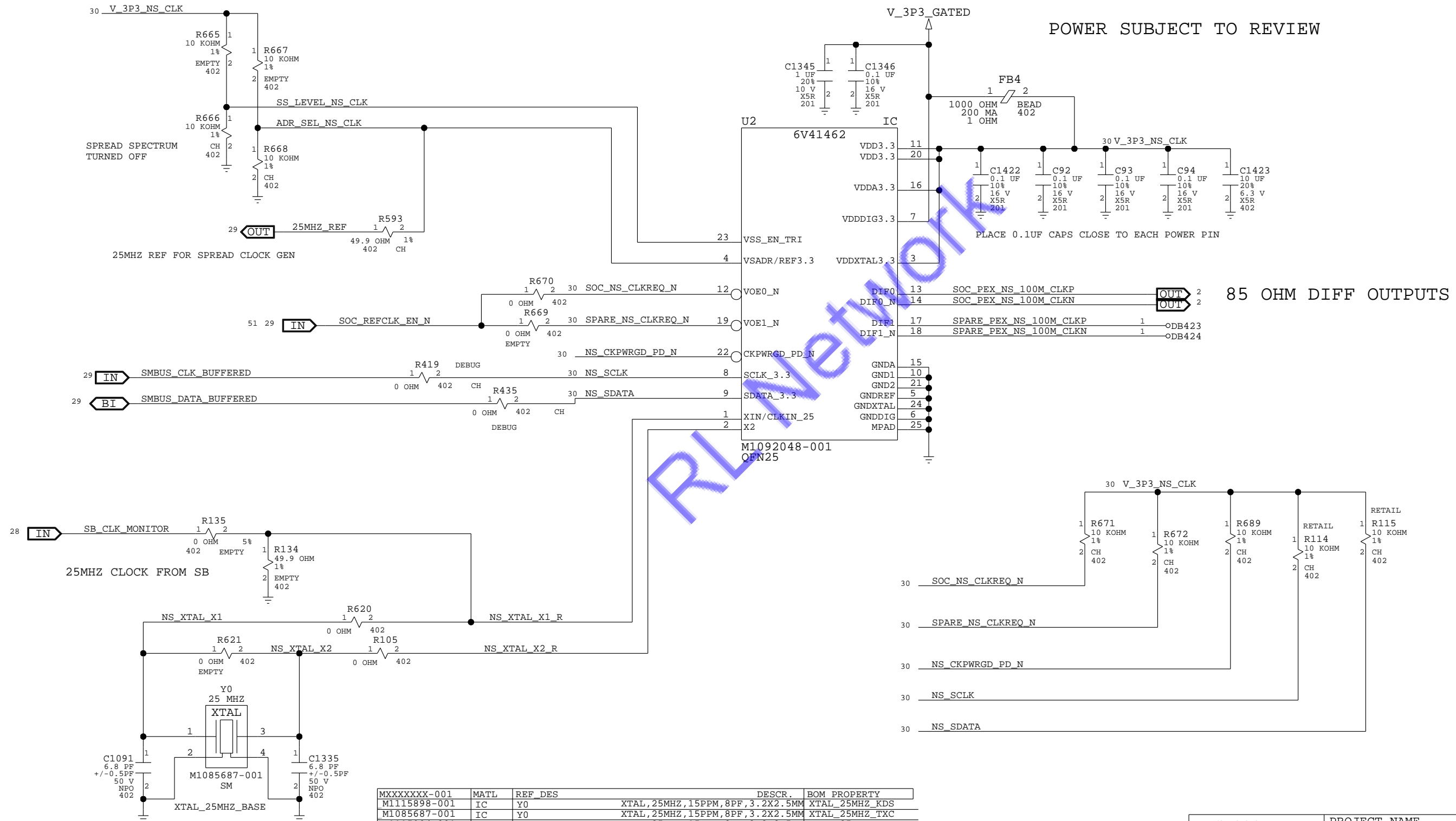


CLOCK: PCIE 100MHZ NS

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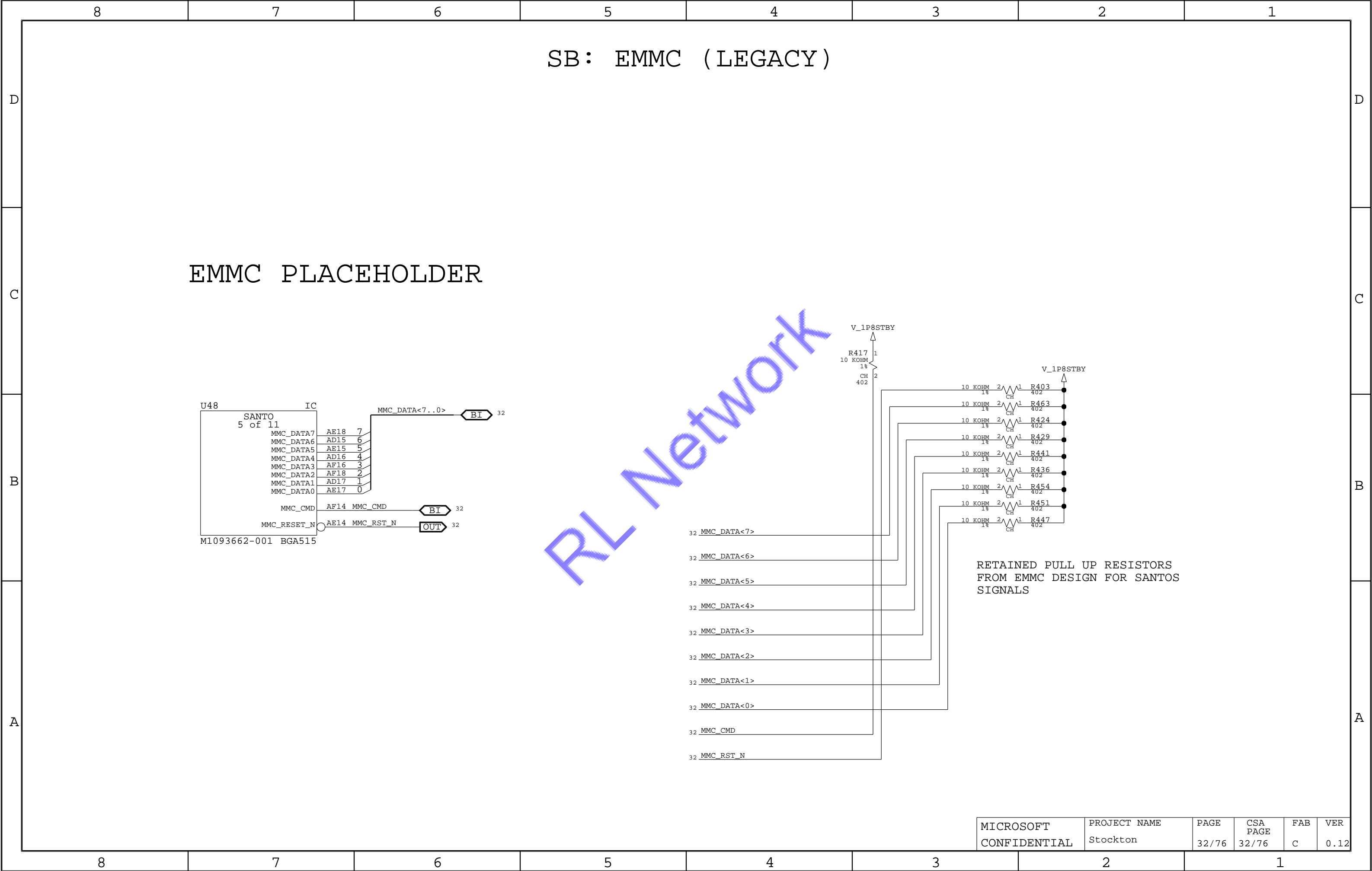
9FGL04 SMBUS ADDRESS
      1101 000  R/W HEX
WRITE 1101 000   0 0XD0
READ  1101 000   1 0XD1

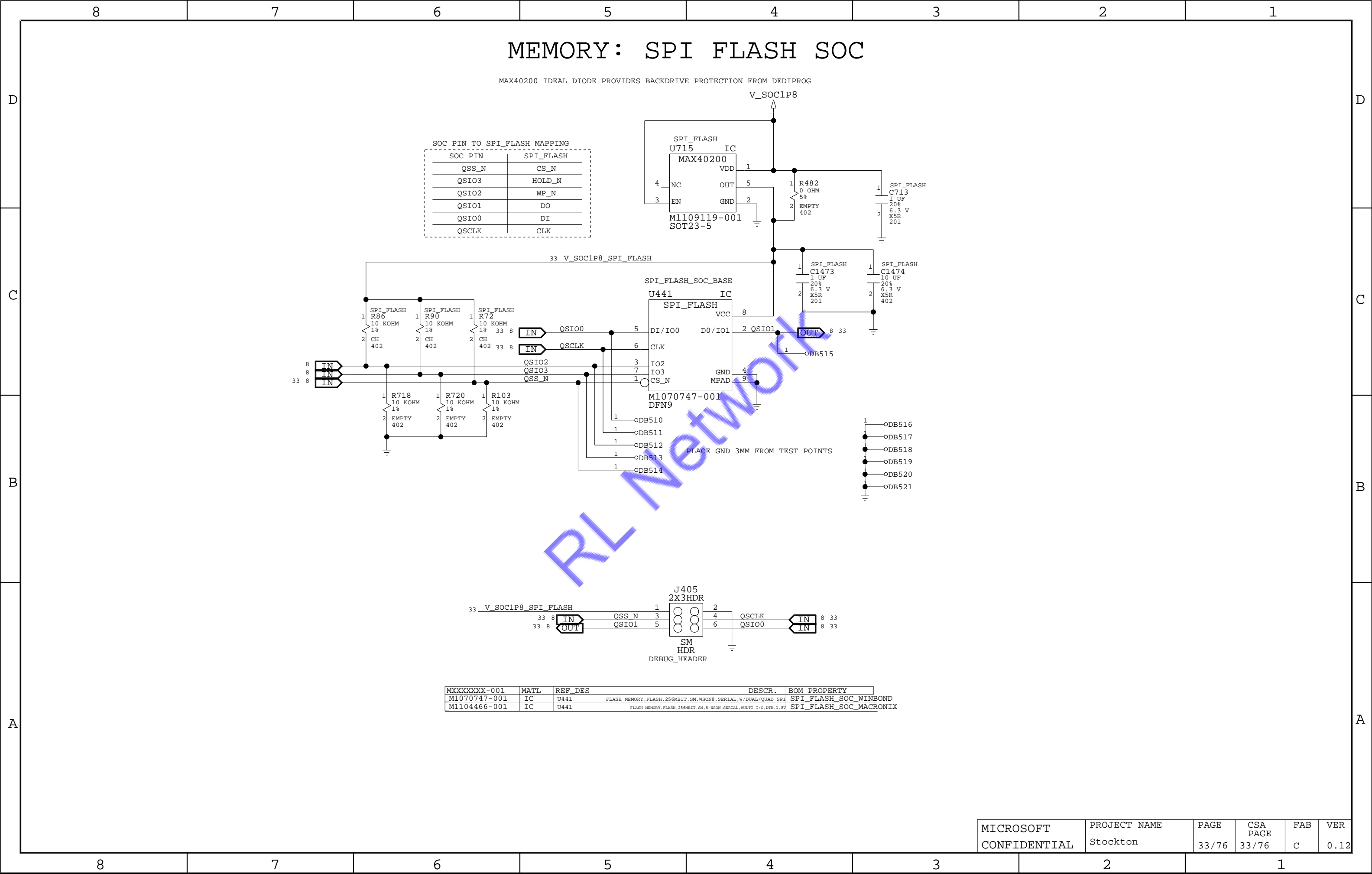
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XXXXXXXX-001	MATL	REF DES	DESCR.	BOM PROPERTY
M115898-001	IC	Y0	XTAL, 25MHZ, 15PPM, 8PF, 3. 2X2.5MM	XTAL_25MHZ_KDS
M1085687-001	IC	Y0	XTAL, 25MHZ, 15PPM, 8PF, 3. 2X2.5MM	XTAL_25MHZ_NDK
M115904-001	IC	Y0	XTAL, 25MHZ, 15PPM, 8PF, 3. 2X2.5MM	XTAL_25MHZ_TXC

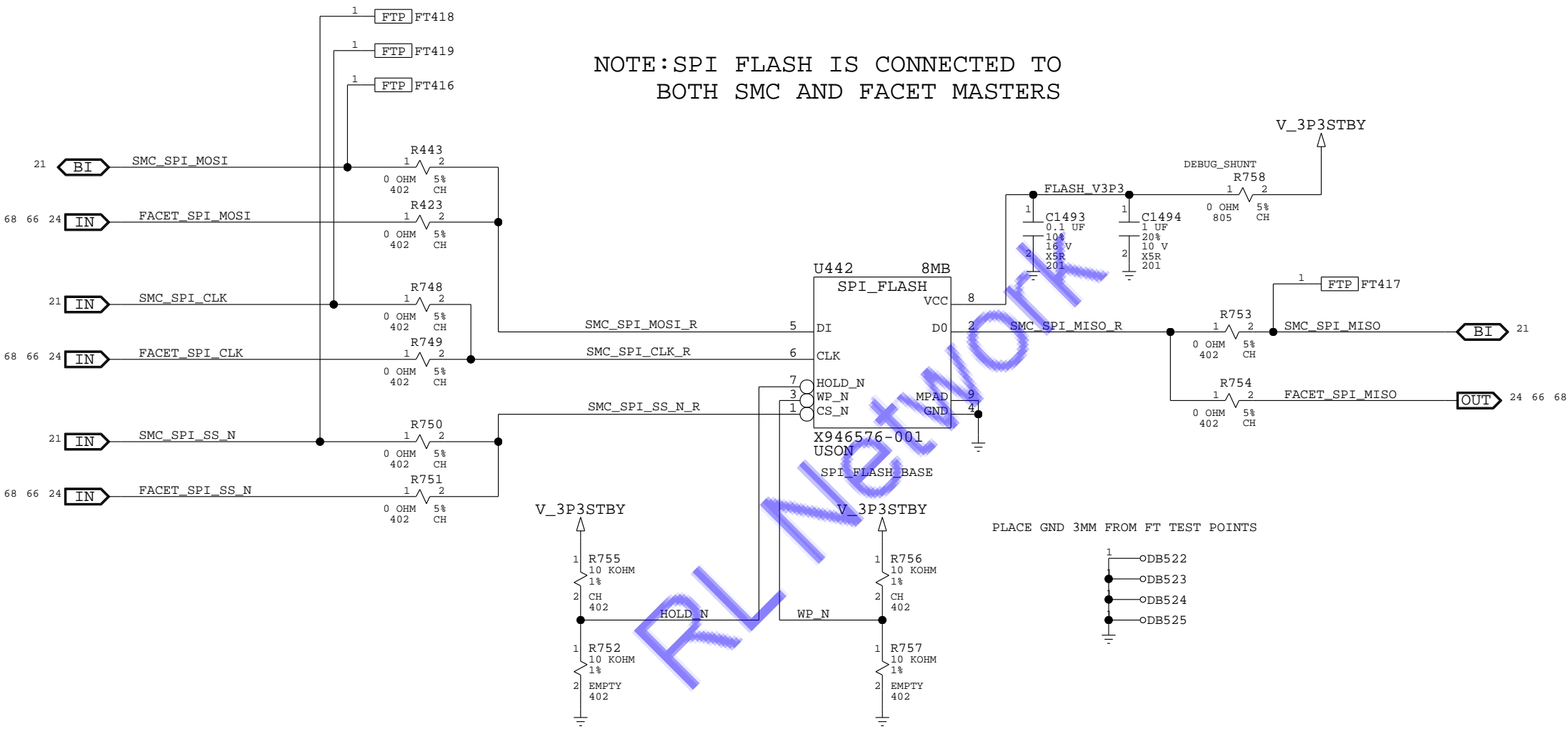




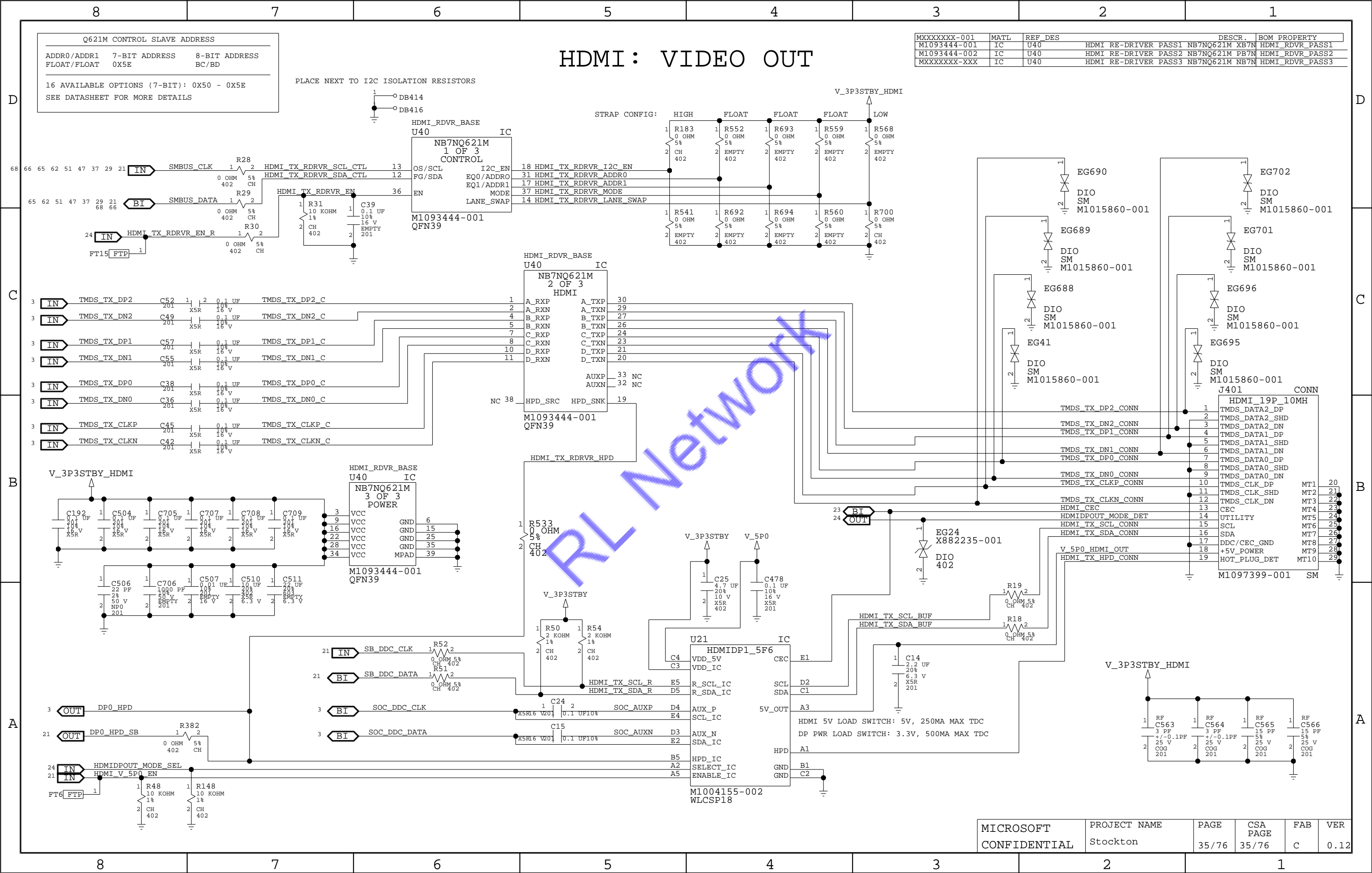


MEMORY: SPI FLASH

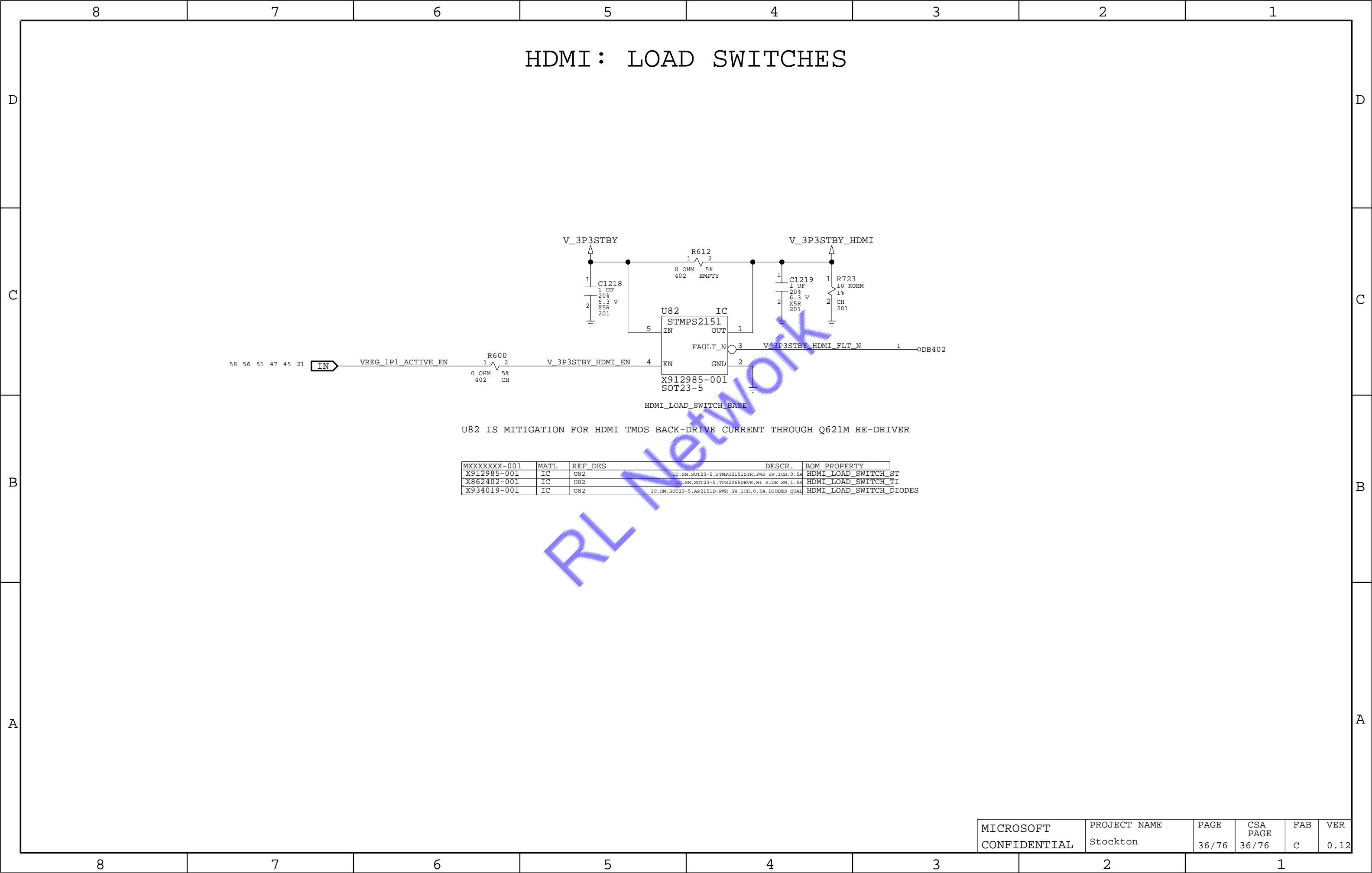
NOTE:SPI FLASH IS CONNECTED TO BOTH SMC AND FACET MASTERS



XXXXXXXX-001	MATL	REF DES	DESCR.	BOM PROPERTY
X946576-001	IC	U442	WINBOND,SPI_FLASH,8GBIT,USON	SPI_FLASH_WINBOND
M1090771-001	IC	U442	MACRONIX,SPI_FLASH,8GBIT,USON	SPI_FLASH_MACRONIX

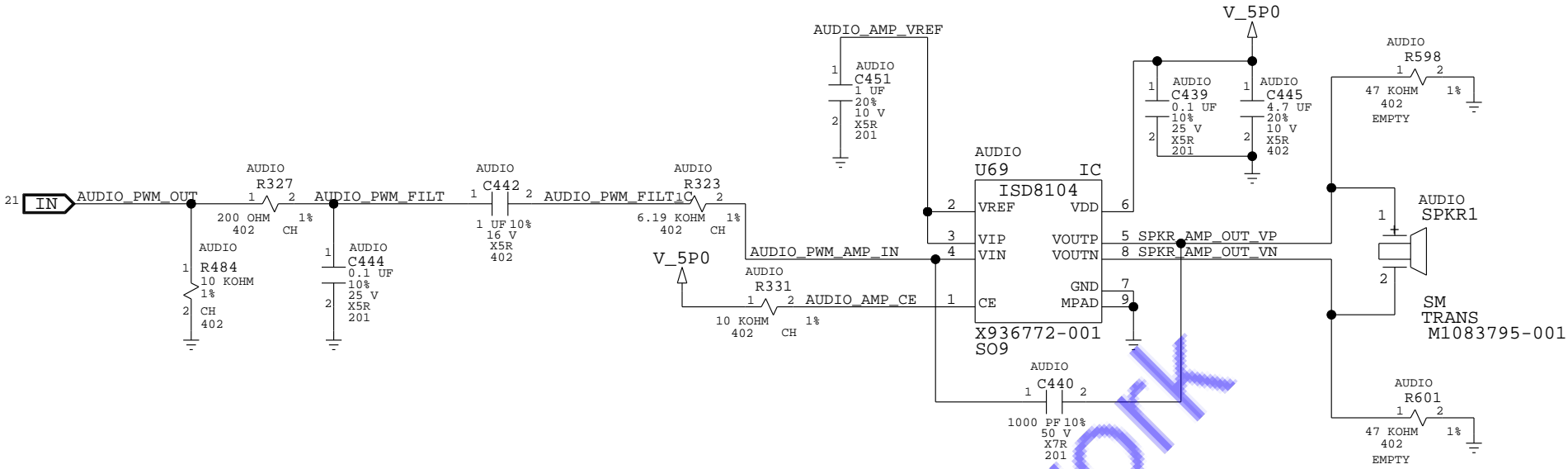


RL Network





AUDIO: PREMIUM AND RETAIL



PREMIUM/SE/LE SKU ONLY



# CONN: RJ45, SPDIF, CFEXPRESS

MXXXXXXX-001	MATL	REF DES	DESCR.	BOM PROPERTY
M1087814-001	CONN	J13	FOXCONN RJ45 CONNECTOR	CON_RJ45_FOXC
MXXXXXXX-001	CONN	J13	AMPHENOL QUAL RJ45 CONNECTOR	CON_RJ45_AMP

D

D

C

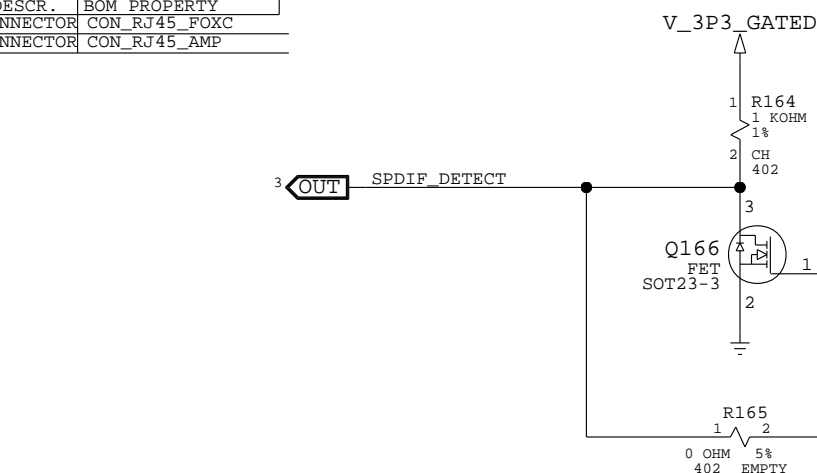
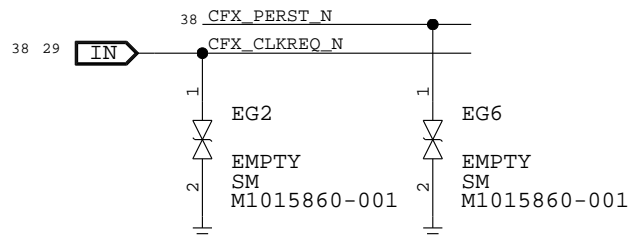
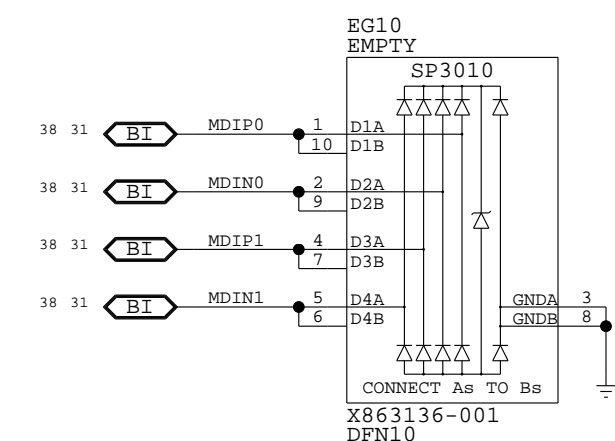
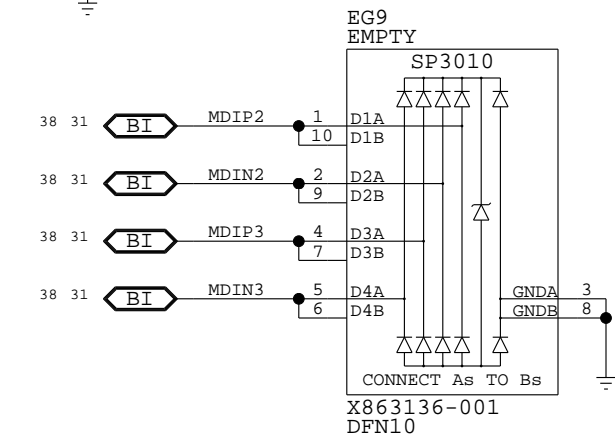
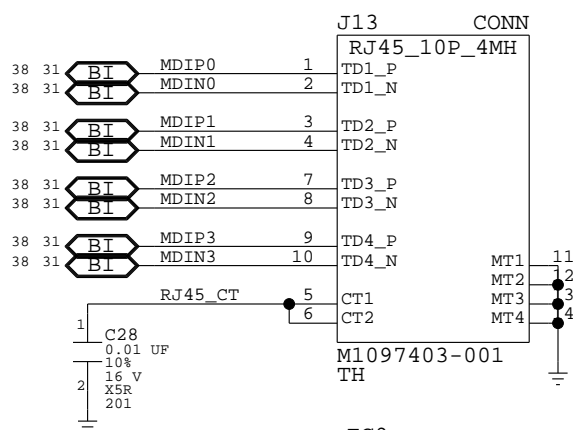
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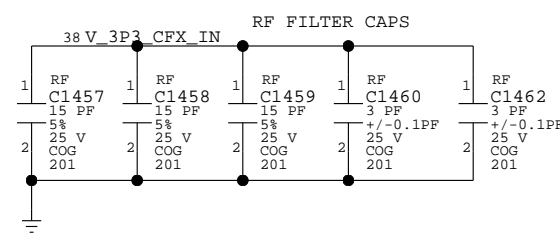
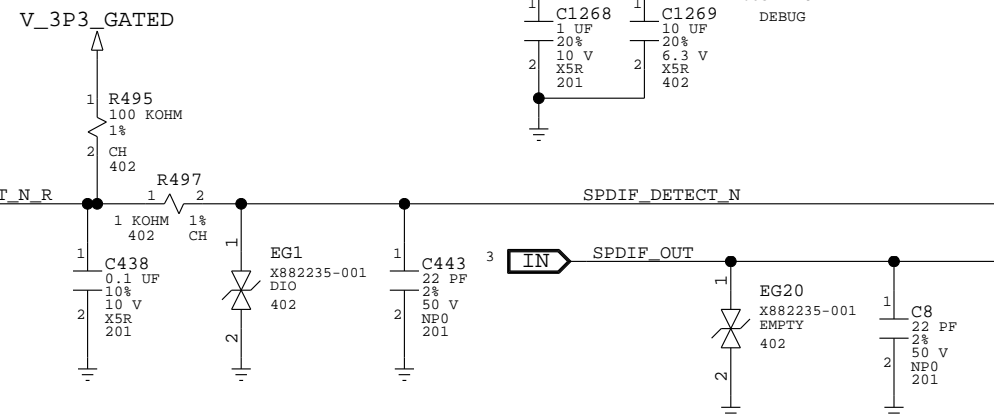
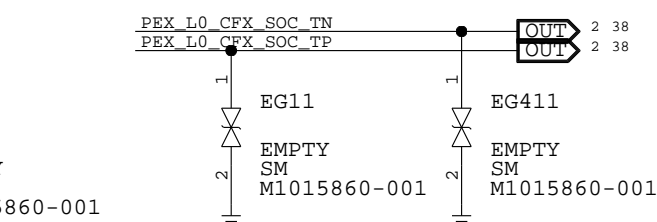
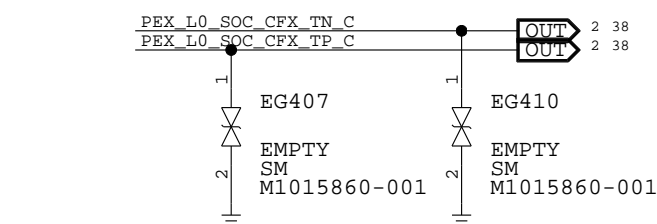
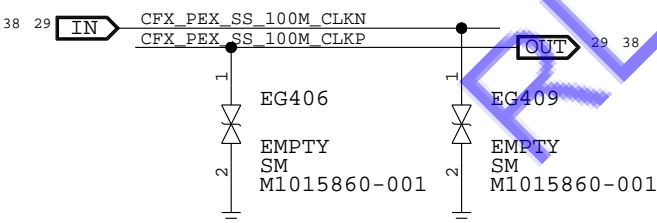
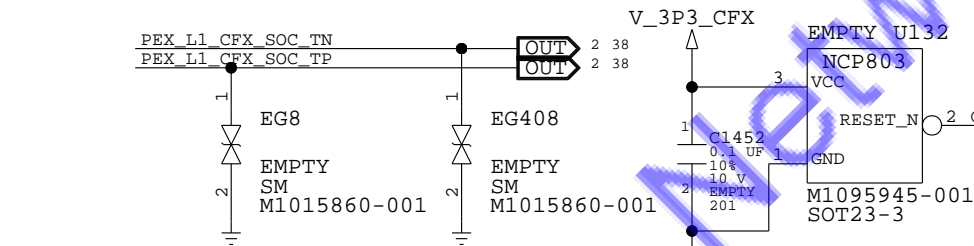
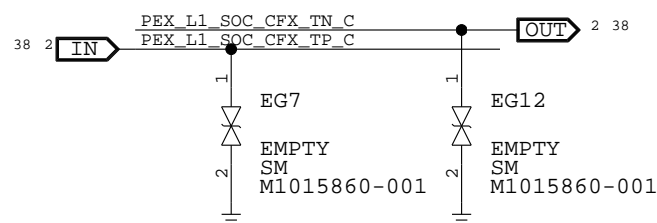
B

A

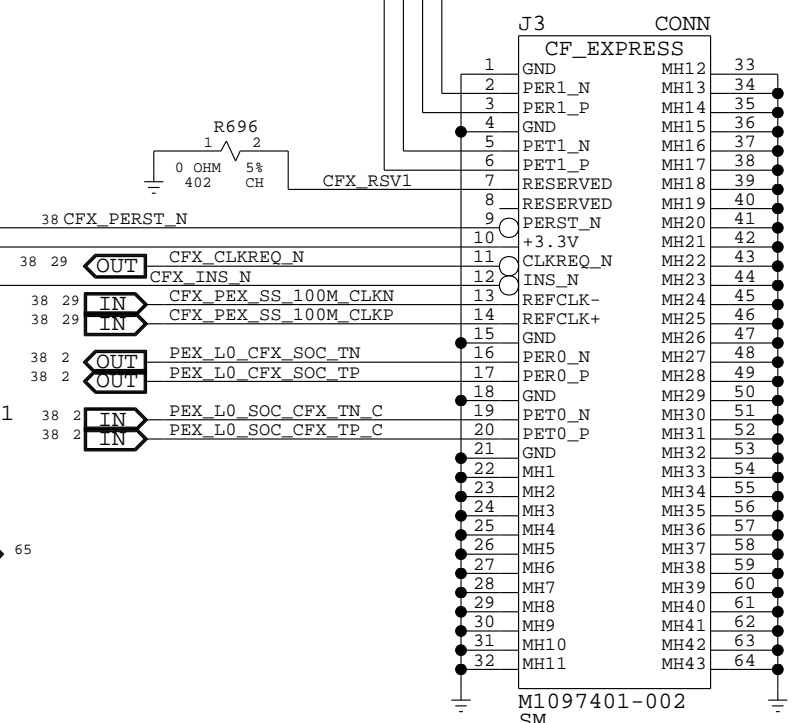
A



Q166 PROVIDES LOGIC INVERSION  
SPDIF DETECT IS ACTIVE LOW  
SOC REQUIRES ACTIVE HIGH



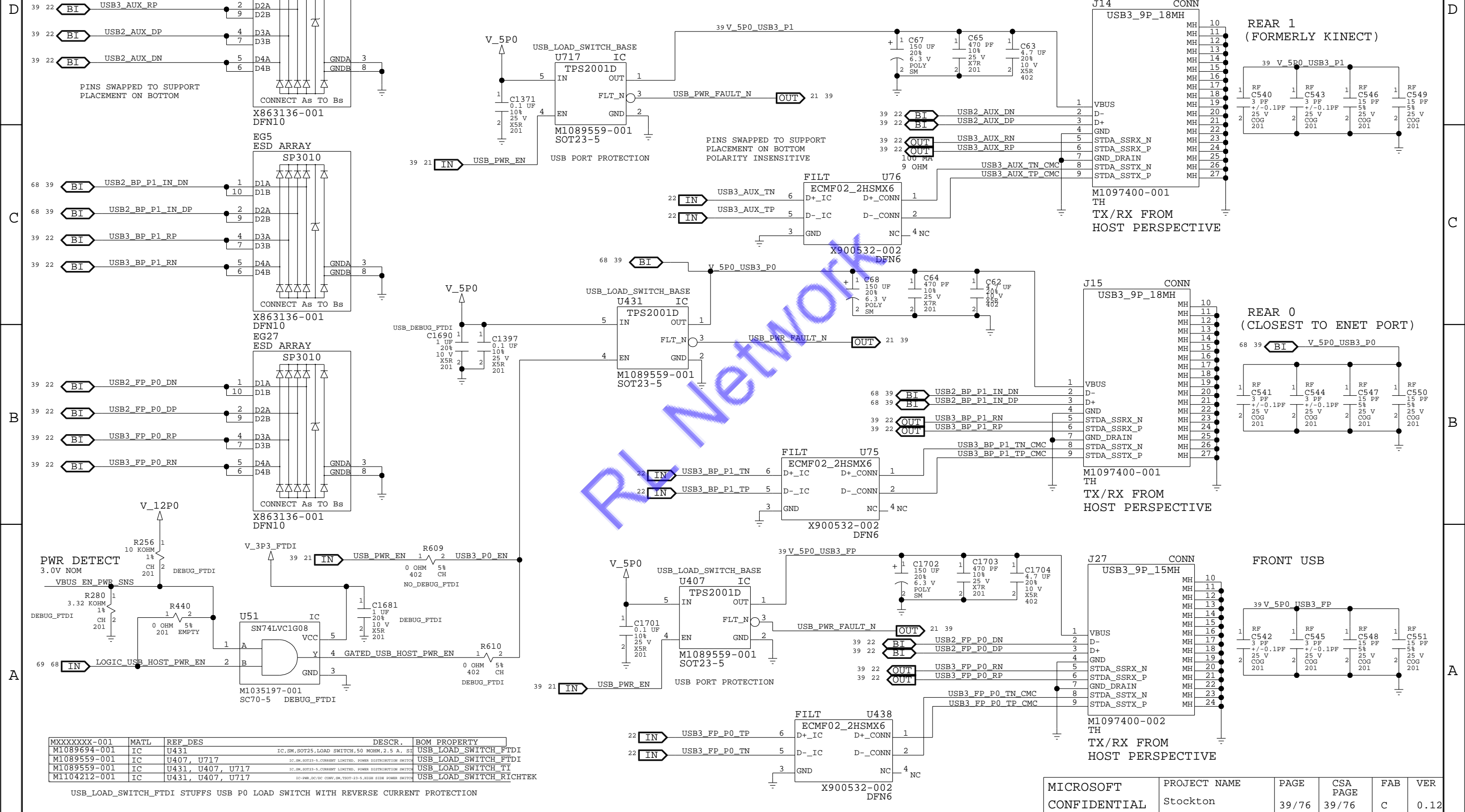
CFEXPRESS  
2.5A EDC  
1.55A TDC



MICROSOFT CONFIDENTIAL	PROJECT NAME Stockton	PAGE 38/76	CSA PAGE 38/76	FAB C	VER 0.12
---------------------------	--------------------------	---------------	----------------------	----------	-------------

# CONN: USB (FRONT & REAR)

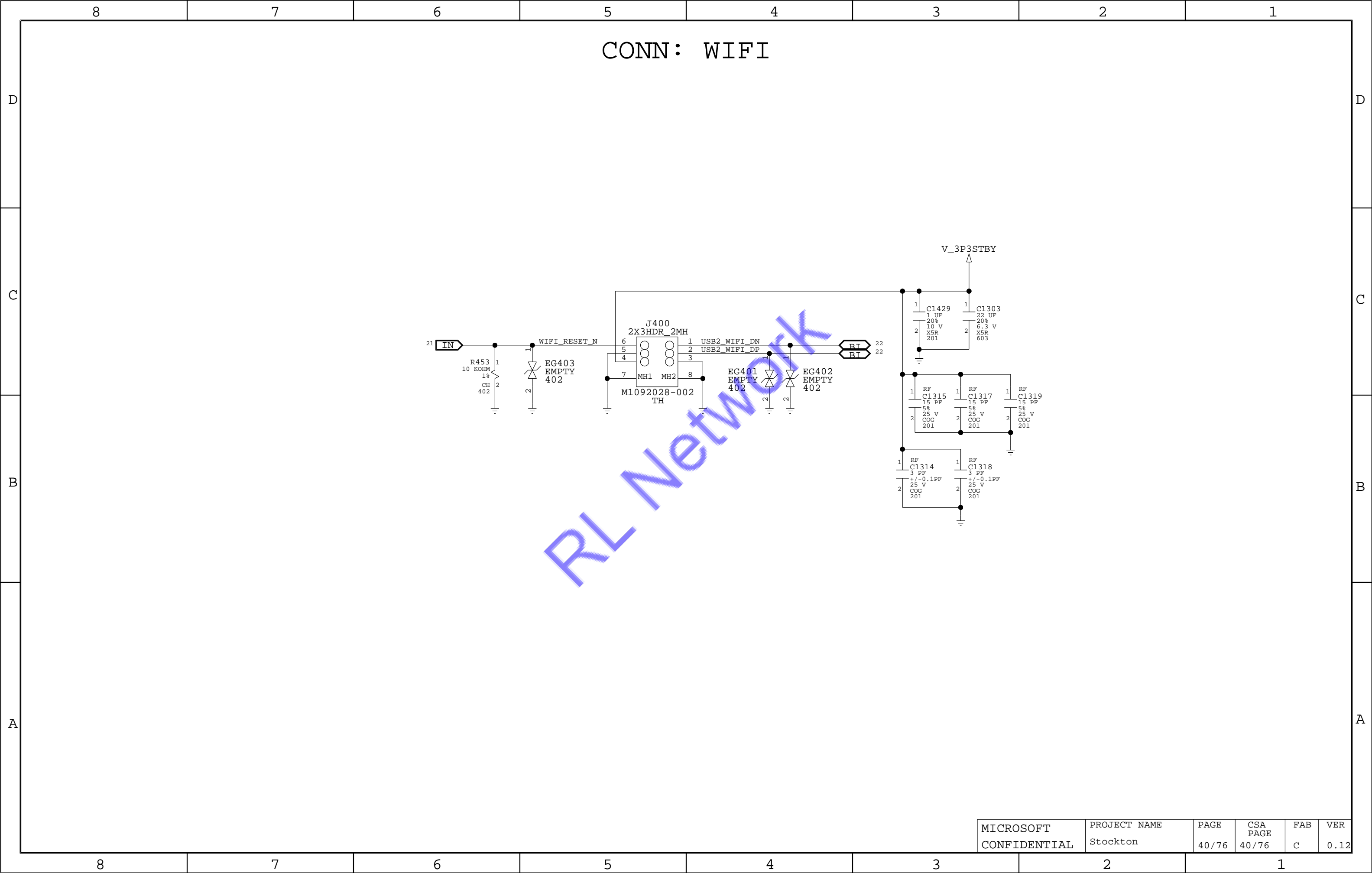
MXXXXXXX-001	MATL	REF DES	DESCR.	BOM PROPERTY
M1087813-001	CONN	J14, J15	FOXCONN USB CONNECTOR	CON_USB_FOXC
MXXXXXXX-001	CONN	J14, J15	AMPHENOL QUAL USB CONNECTOR	CON_USB_AMP



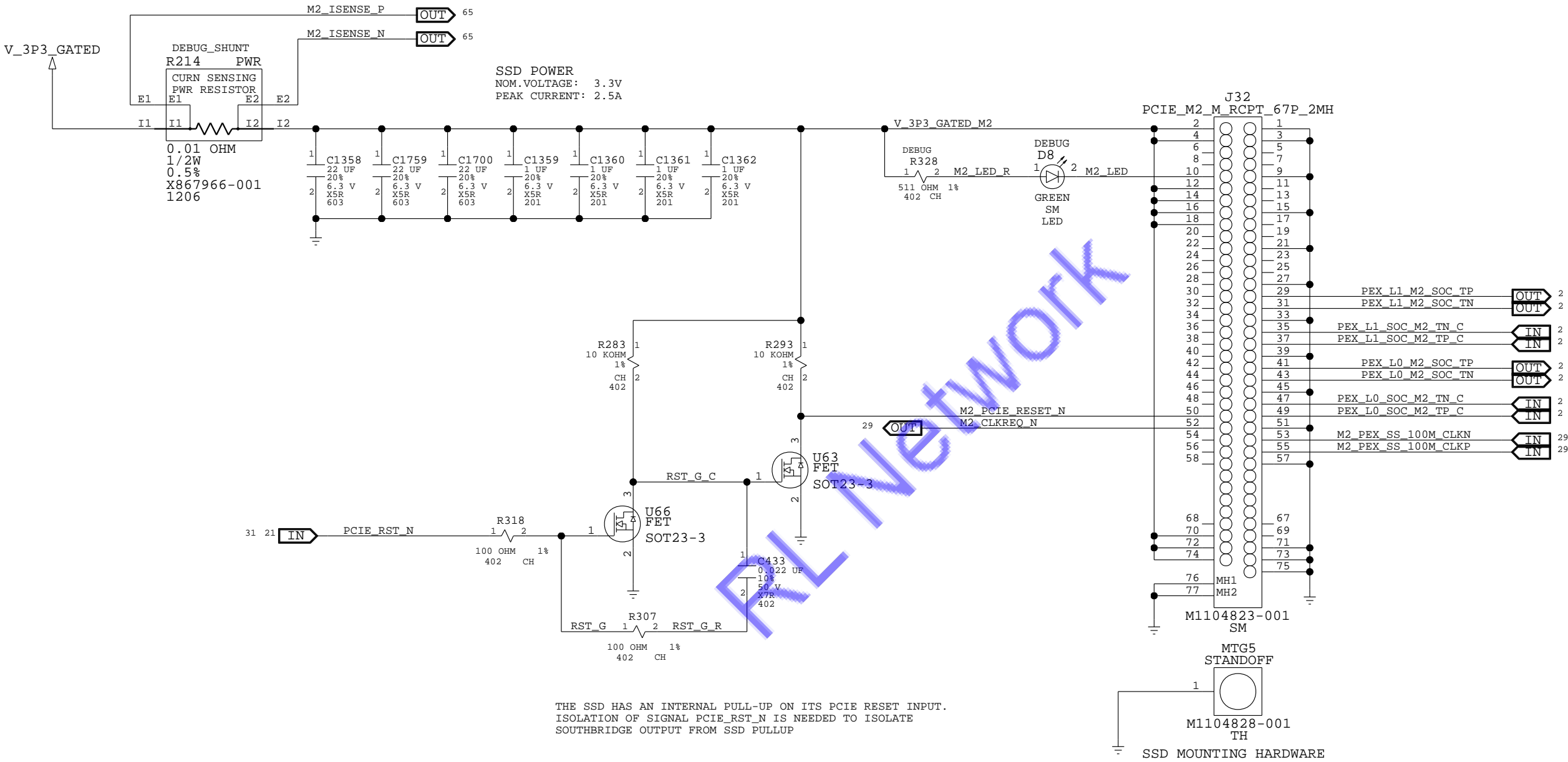
MXXXXXXX-001	MATL	REF DES	DESCR.	BOM PROPERTY
M1089694-001	IC	U431	IC, SM, SOT23, LOAD SWITCH, 50 MOHM, 2.5 A, 50	USB_LOAD_SWITCH_FTDI
M1089559-001	IC	U407, U717	IC, SM, SOT23-5, CURRENT LIMITED, POWER DISTRIBUTION SWITCH	USB_LOAD_SWITCH_FTDI
M1089559-001	IC	U431, U407, U717	IC, SM, SOT23-5, CURRENT LIMITED, POWER DISTRIBUTION SWITCH	USB_LOAD_SWITCH_TI
M1104212-001	IC	U431, U407, U717	IC, PMB, DC/DC CONV, SM, TQFP-23-5, HIGH SIDE POWER SWITCH	USB_LOAD_SWITCH_RICHTK

USB\_LOAD\_SWITCH\_FTDI STUFFS USB P0 LOAD SWITCH WITH REVERSE CURRENT PROTECTION

MICROSOFT	PROJECT NAME	PAGE	CSA	FAB	VER
CONFIDENTIAL	Stockton	39/76	PAGE 39/76	C	0.12



CONN: M.2

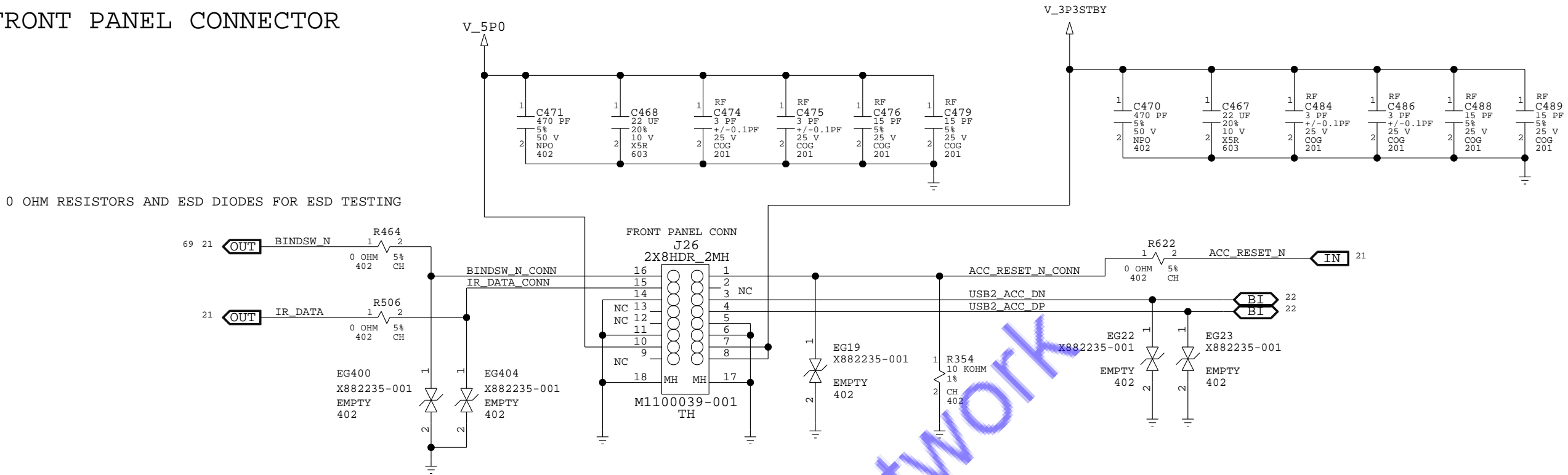


POLARITY SWAPPED TO SUPPORT  
ROUTING ON TWO SIDES OF BOARD

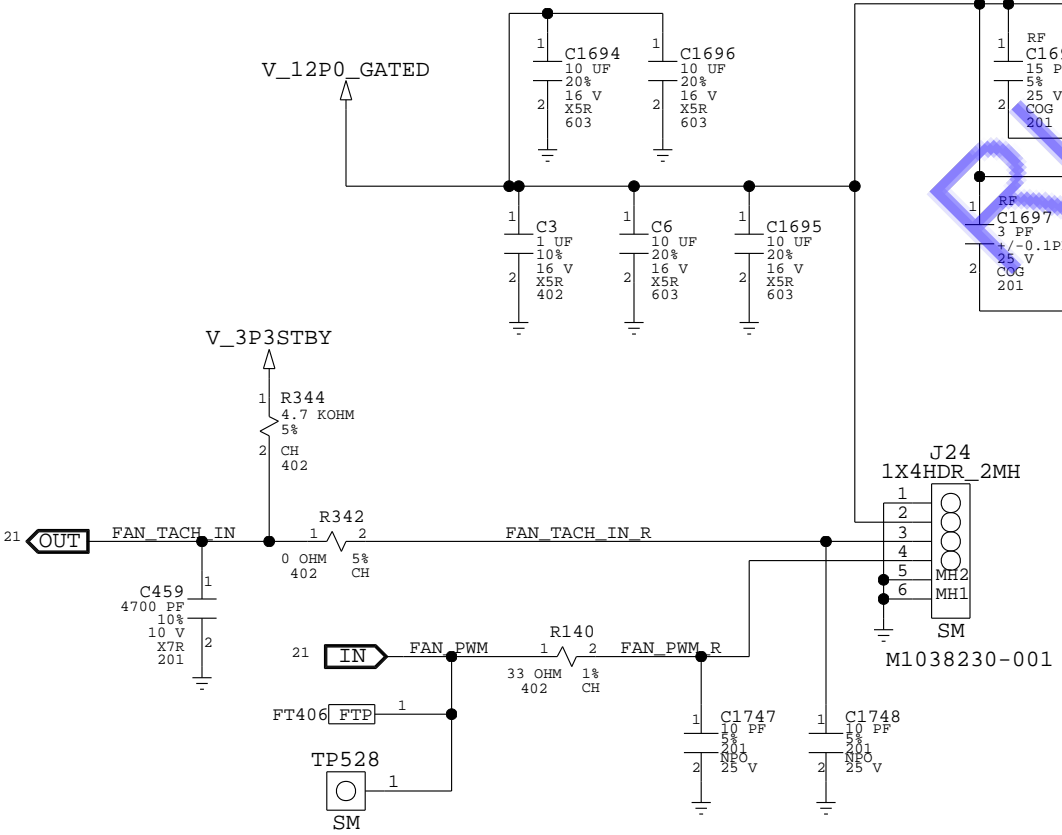
8		7		6		5		4		3		2		1	
CONN: ODD															
PLACEHOLDER FOR OBSOLETE ODD CIRCUITRY															
RL Network															
MICROSOFT CONFIDENTIAL															
PROJECT NAME Stockton															
PAGE 42/76															
CSA PAGE 42/76															
FAB C															
VER 0.12															
8		7		6		5		4		3		2		1	

CONN: FRONT PANEL, FAN, NEXUS

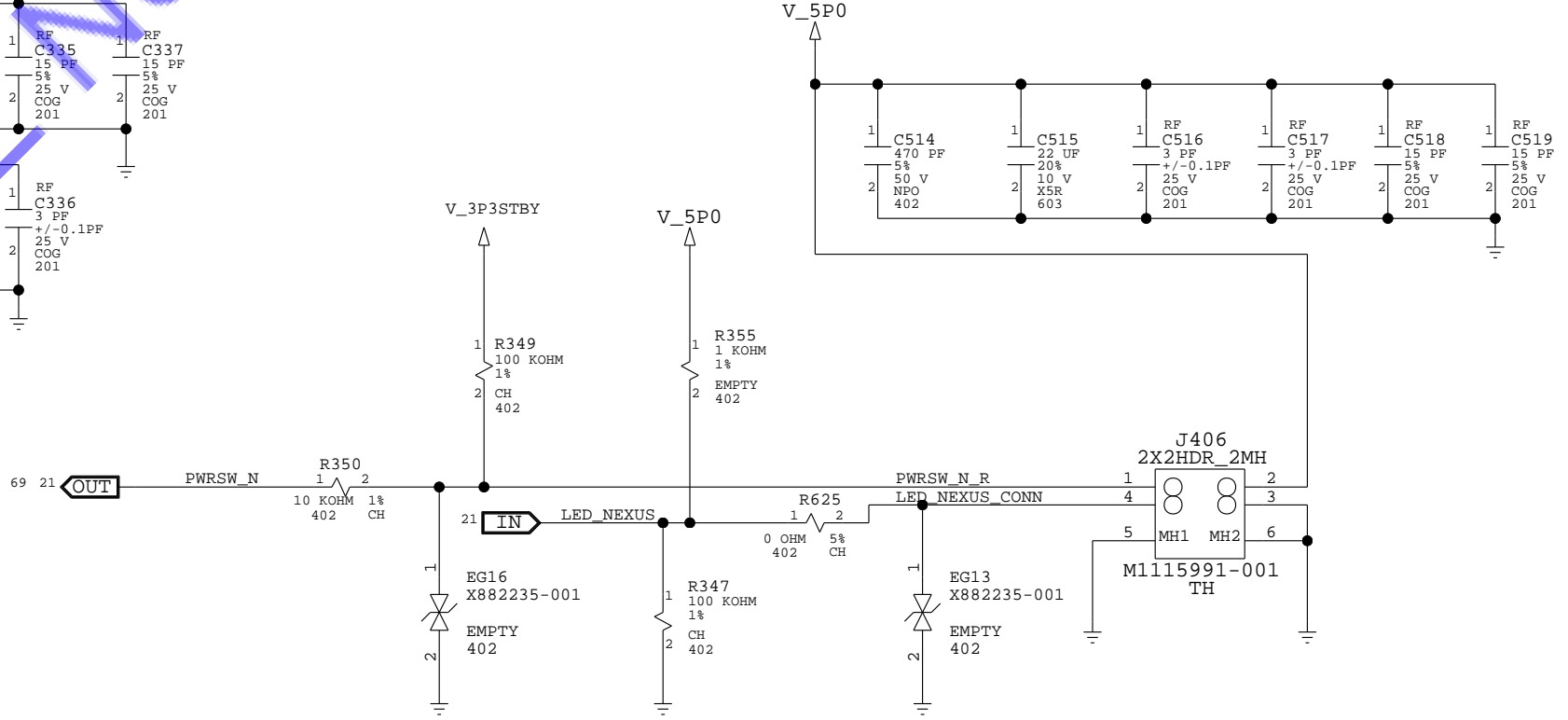
FRONT PANEL CONNECTOR



FAN CONNECTOR

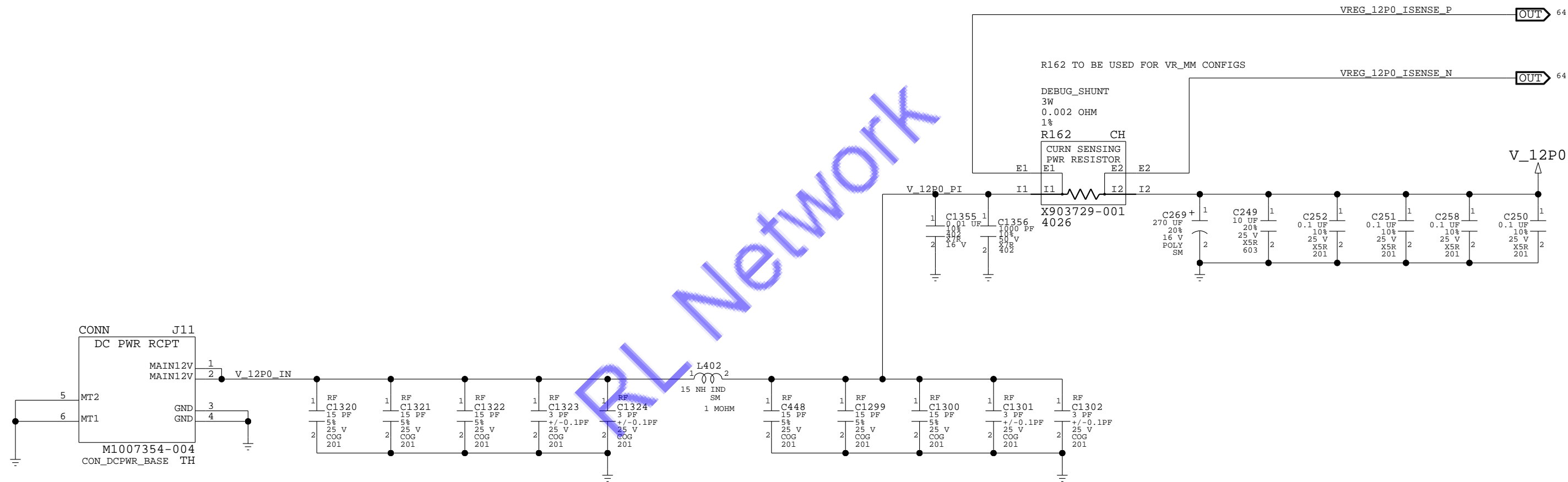


NEXUS CONNECTOR

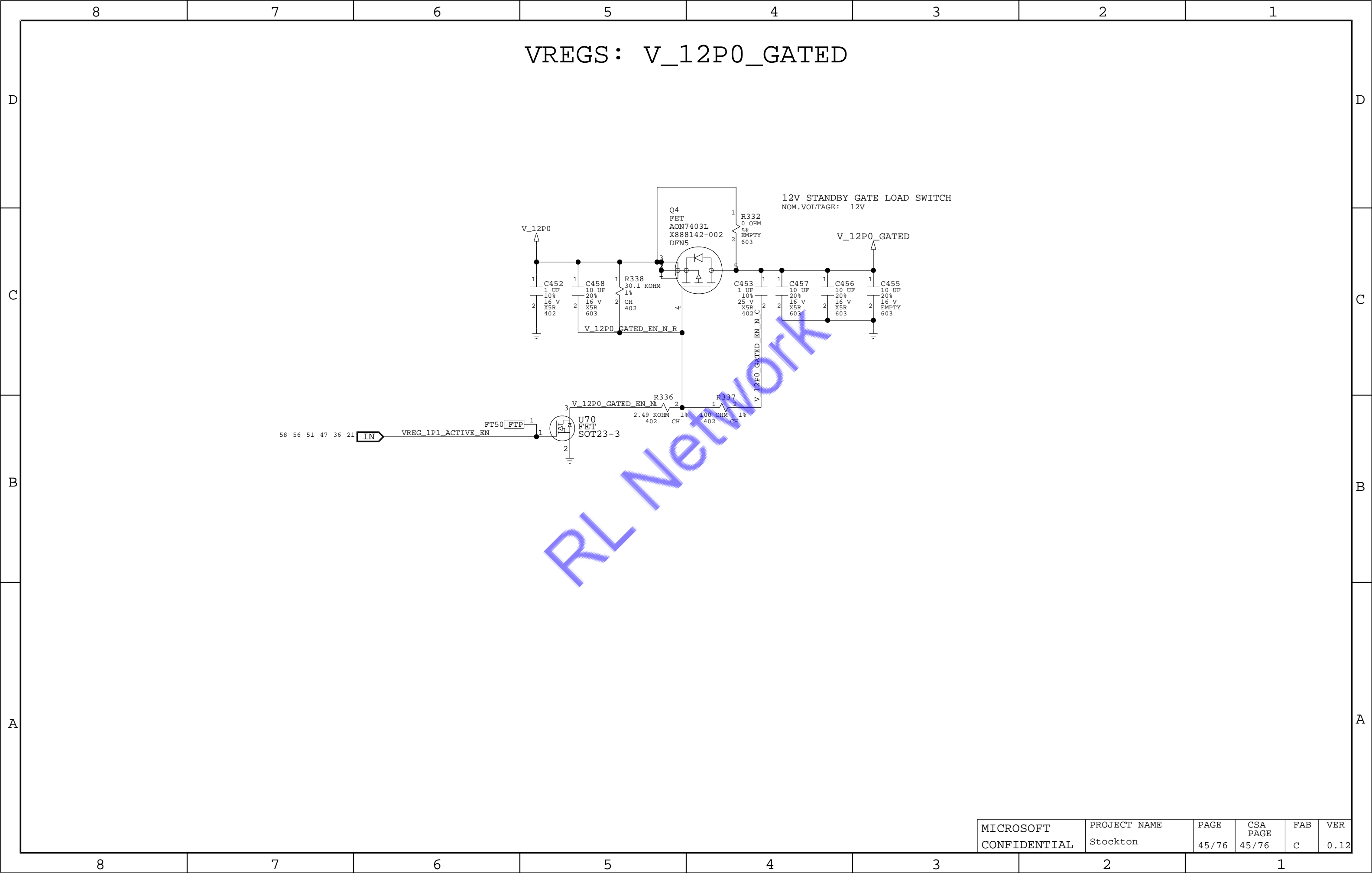




CONN: POWER

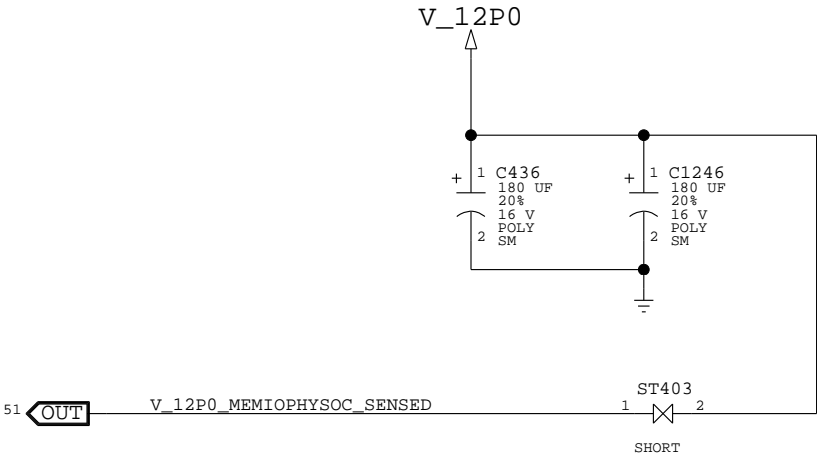


MXXXXXXX-001	MATL	REF	DES	DESCR.	BOM PROPERTY
M1007354-004	CONN	J11	FOXCONN DC POWER CONNECTOR 1ST MAT SRC	CON_DCPWR_FOXC_1	
M1021821-003	CONN	J11	FOXLINK QUAL DC POWER CONN 1ST MAT SRC	CON_DCPWR_FOXL_1	
M1040539-001	CONN	J11	FOXCONN QUAL DC POWER CONN 2ND MAT SRC	CON_DCPWR_FOXC_2	
M1040540-001	CONN	J11	FOXLINK QUAL DC POWER CONN 2ND MAT SRC	CON_DCPWR_FOXL_2	

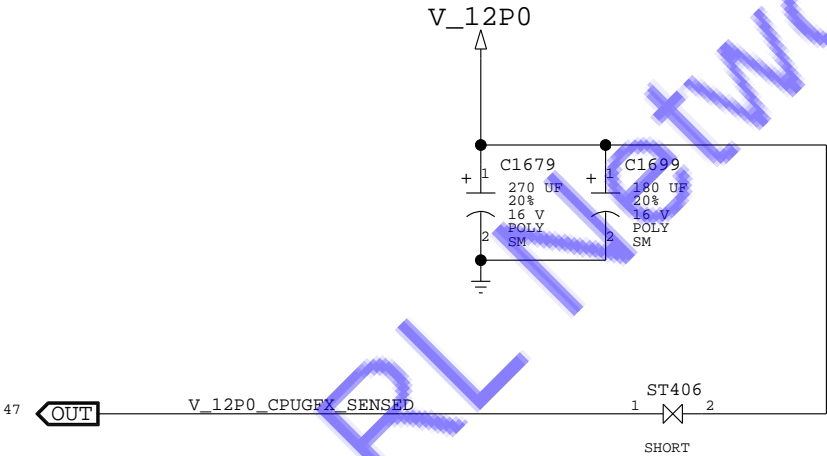


VREGS: INPUT DECOUPLING

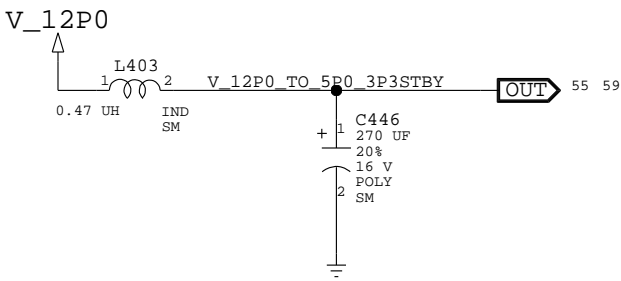
CPU/MEMIO/MEMPHY/SOC INPUT FILTER



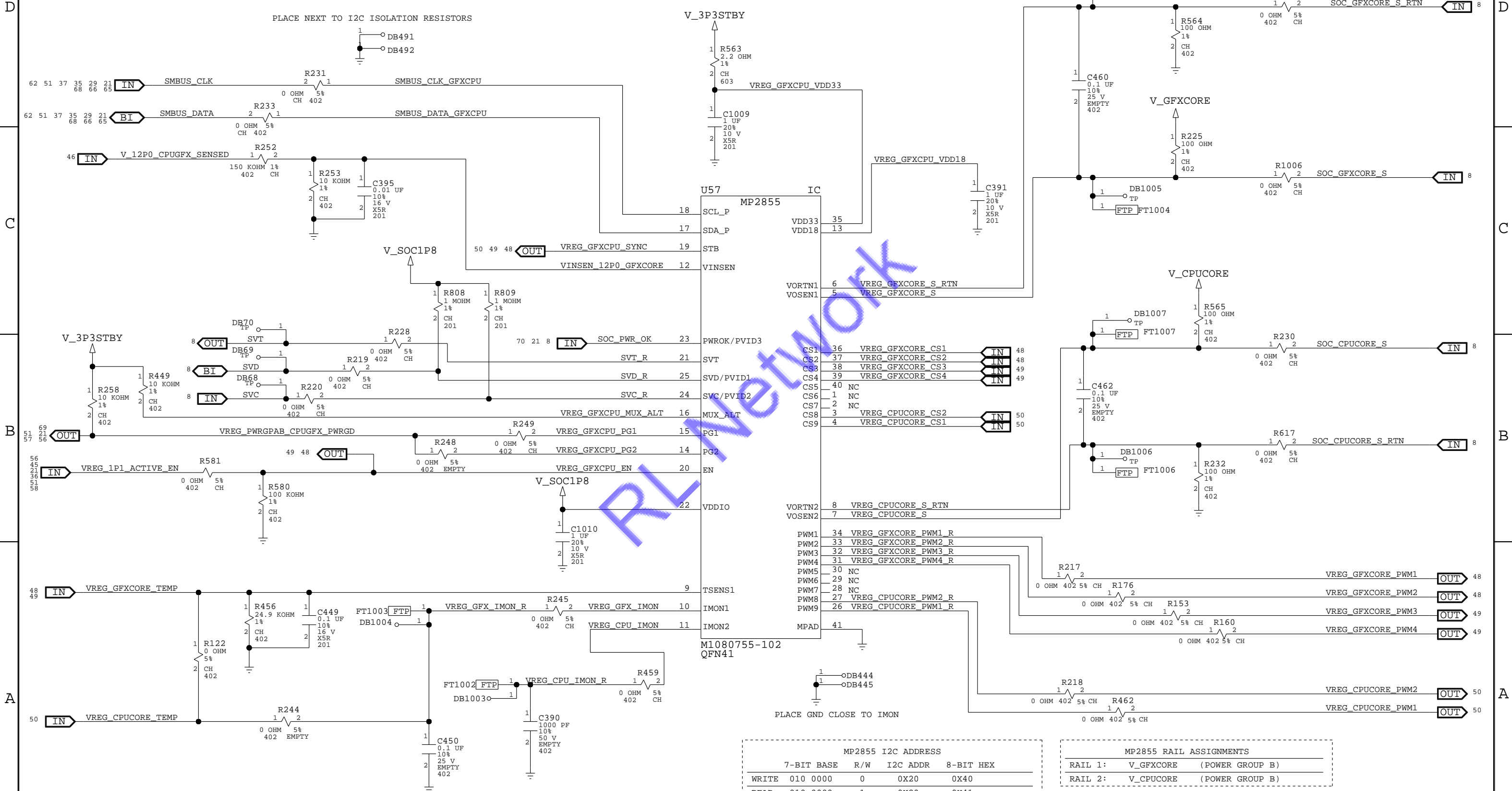
GFX INPUT FILTER



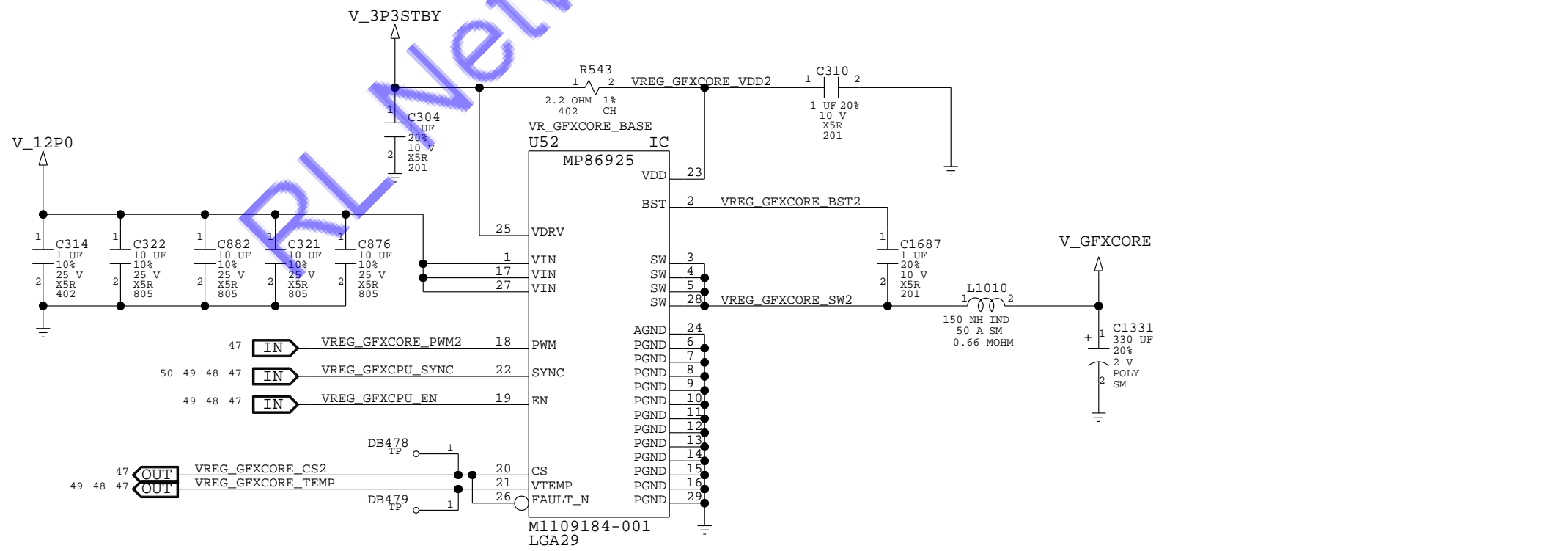
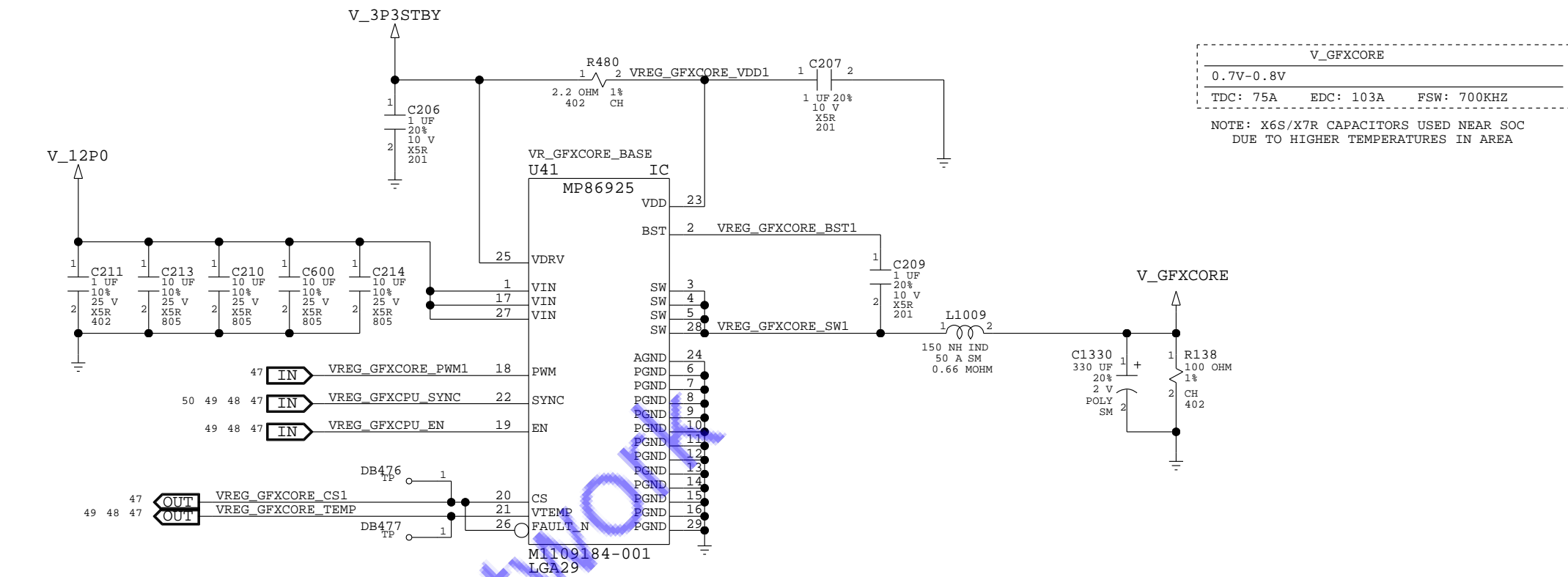
5P0 AND 3P3STBY INPUT FILTER



VREGS: V\_CPUCORE, V\_GFXCORE CONTROLLER

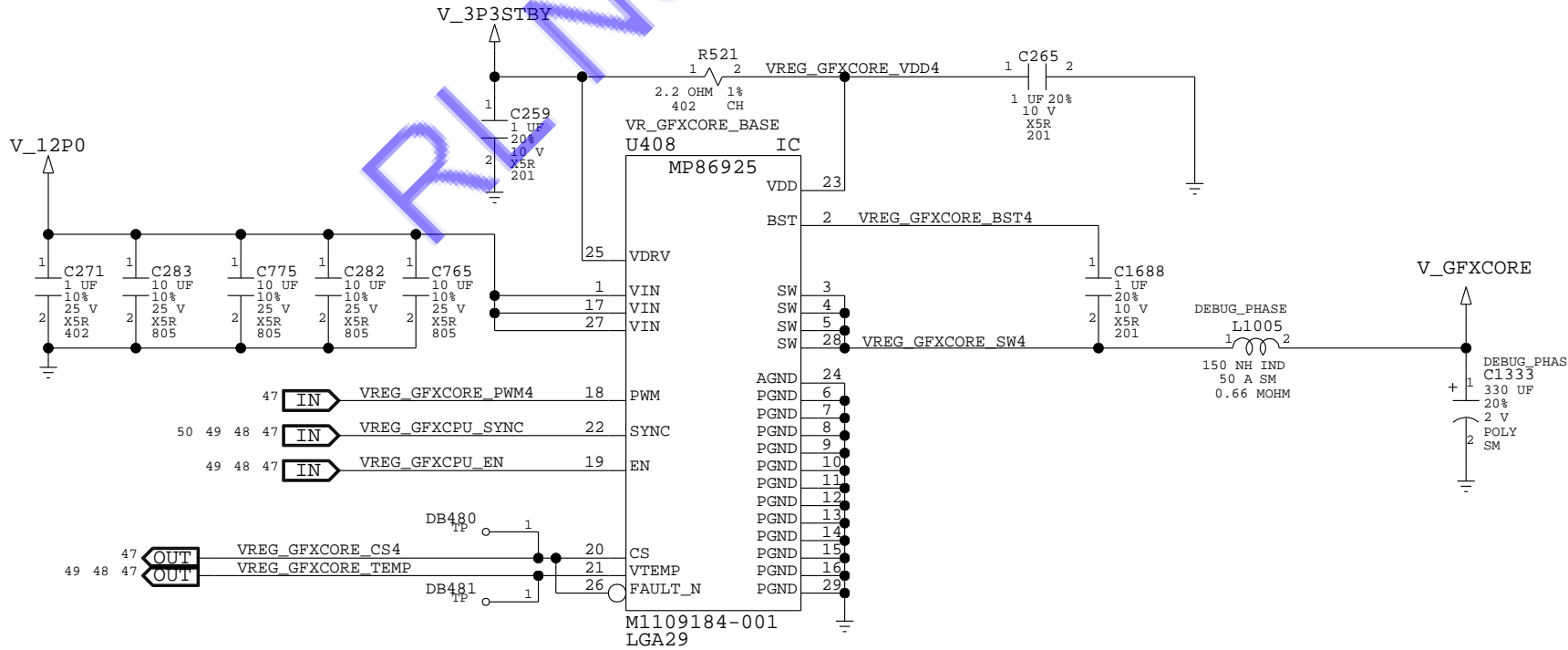
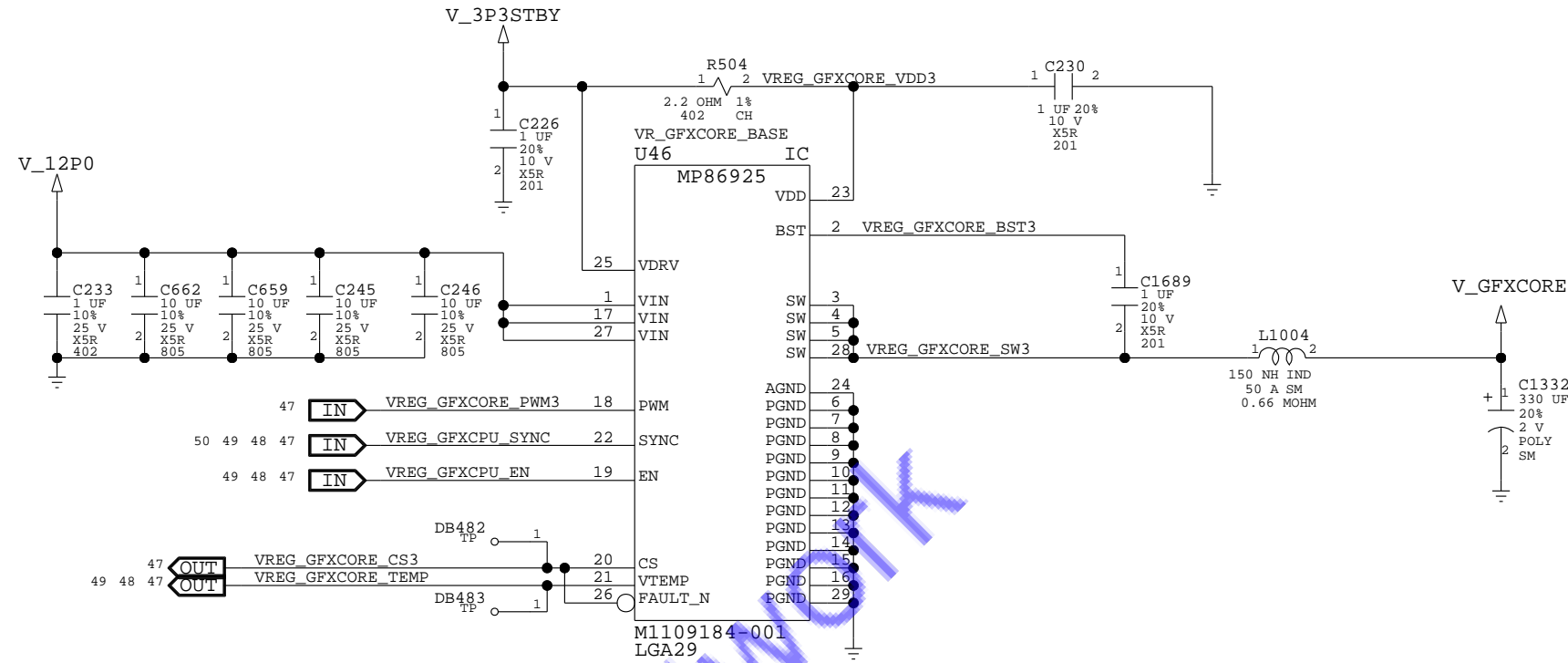


VREGS: V\_GFXCORE OUTPUT PHASE 1 & 2

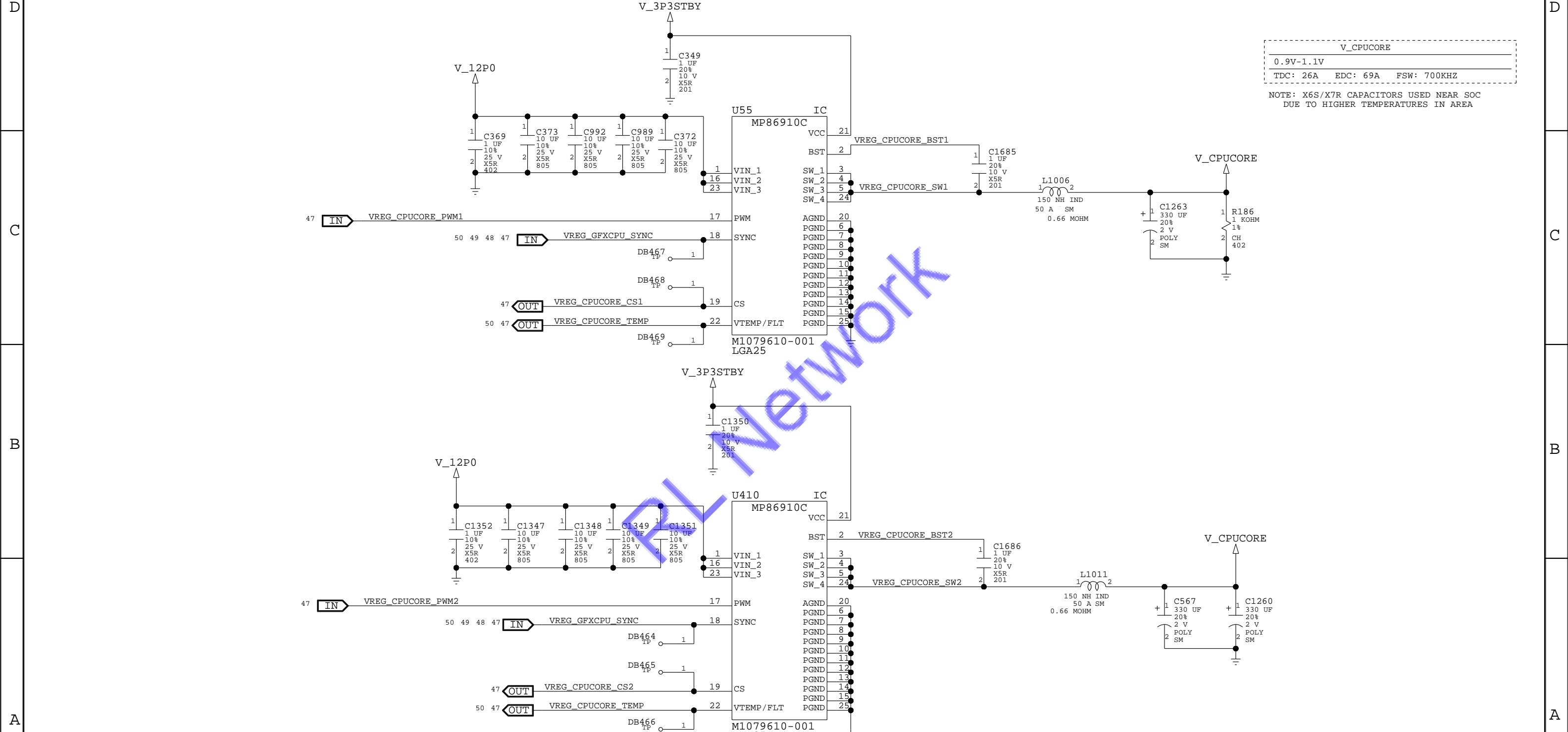


MXXXXXXX-001	MATL	REF DES	DESCR.	BOM PROPERTY
M1109184-001	IC	U41, U52, U46, U408	IC-PWR, DC/DC CONV, MP86925	VR_GFXCORE_MP86925
M1079609-001	IC	U41, U52, U46, U408	IC-PWR, DC/DC CONV, MP86915	VR_GFXCORE_MP86915
M1109184-001	IC	U41, U52, U46	IC-PWR, DC/DC CONV, MP86925	VR_GFXCORE_RETAIL

VREGS: V\_GFXCORE OUTPUT PHASE 3 & 4

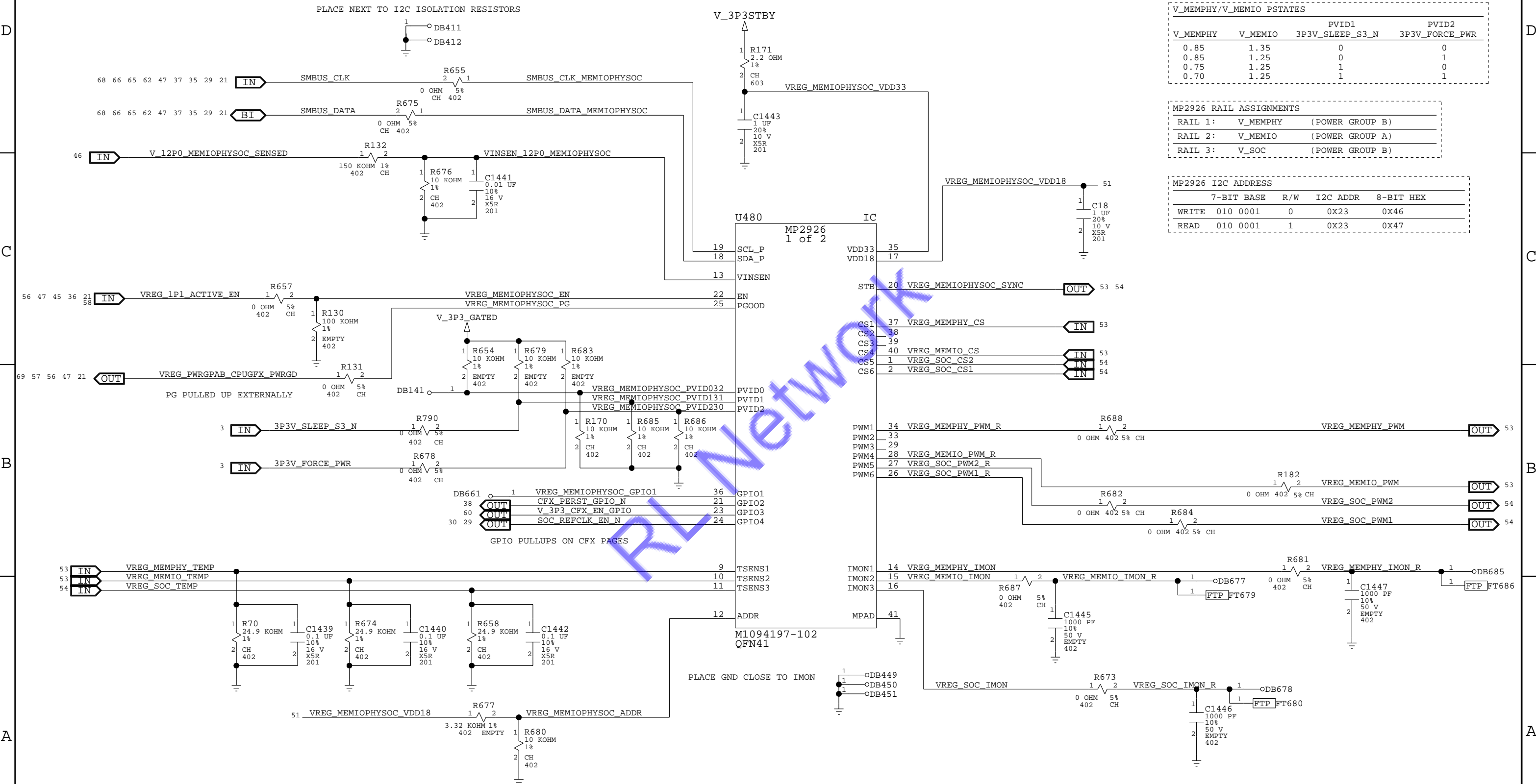


8	7	6	5	4	3	2	1
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```
VREGS:  V_MEMIO,  V_MEMPHY,  V_SOC  CONTROLLER
```

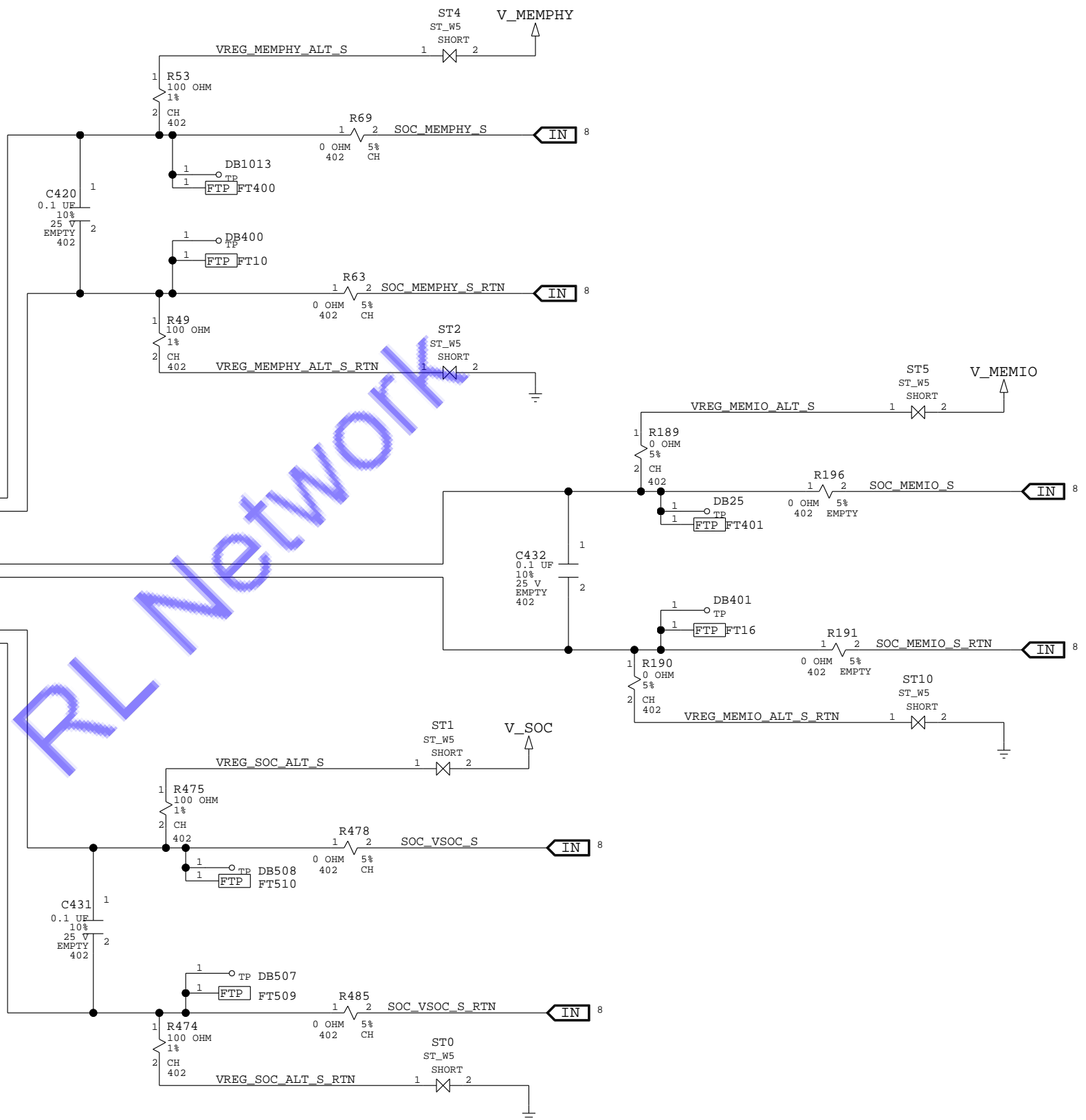
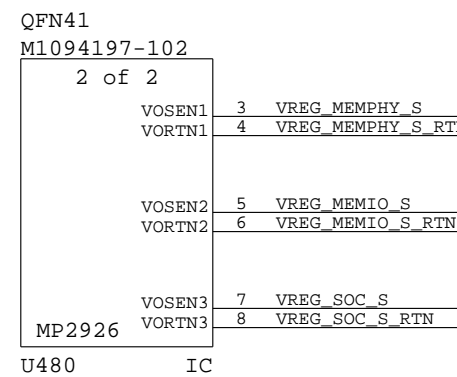


V_MEMPHY/V_MEMIO PSTATES			
V_MEMPHY	V_MEMIO	PVID1 3P3V_SLEEP_S3_N	PVID2 3P3V_FORCE_PWR
0.85	1.35	0	0
0.85	1.25	0	1
0.75	1.25	1	0
0.70	1.25	1	1

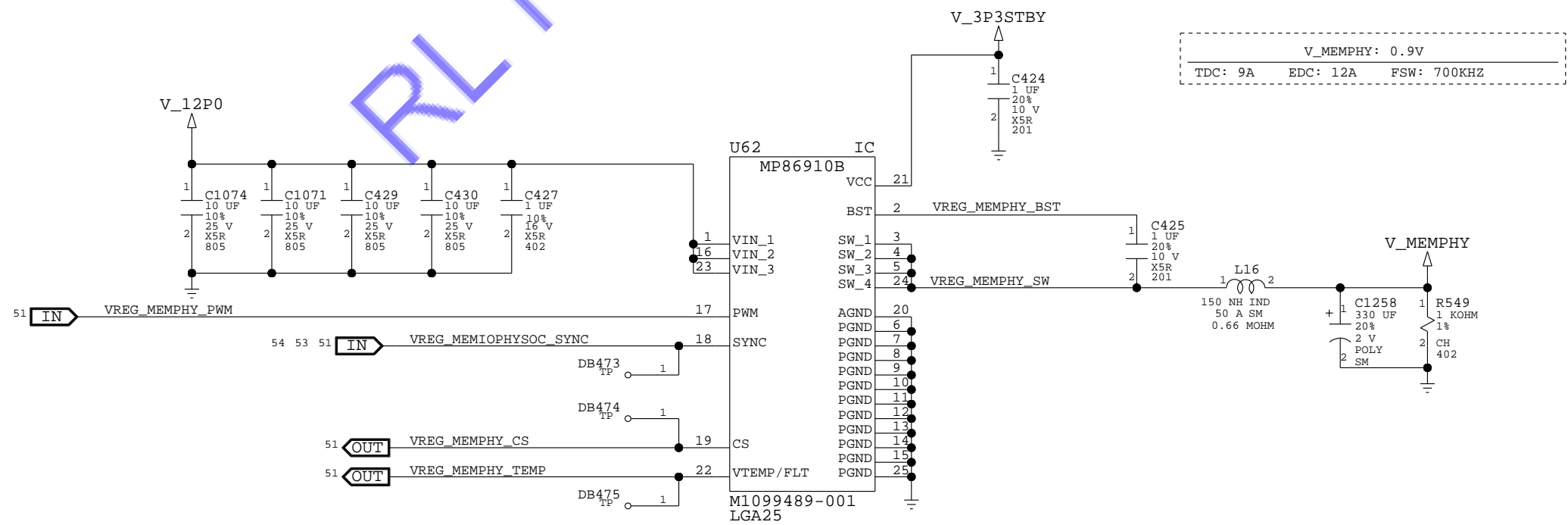
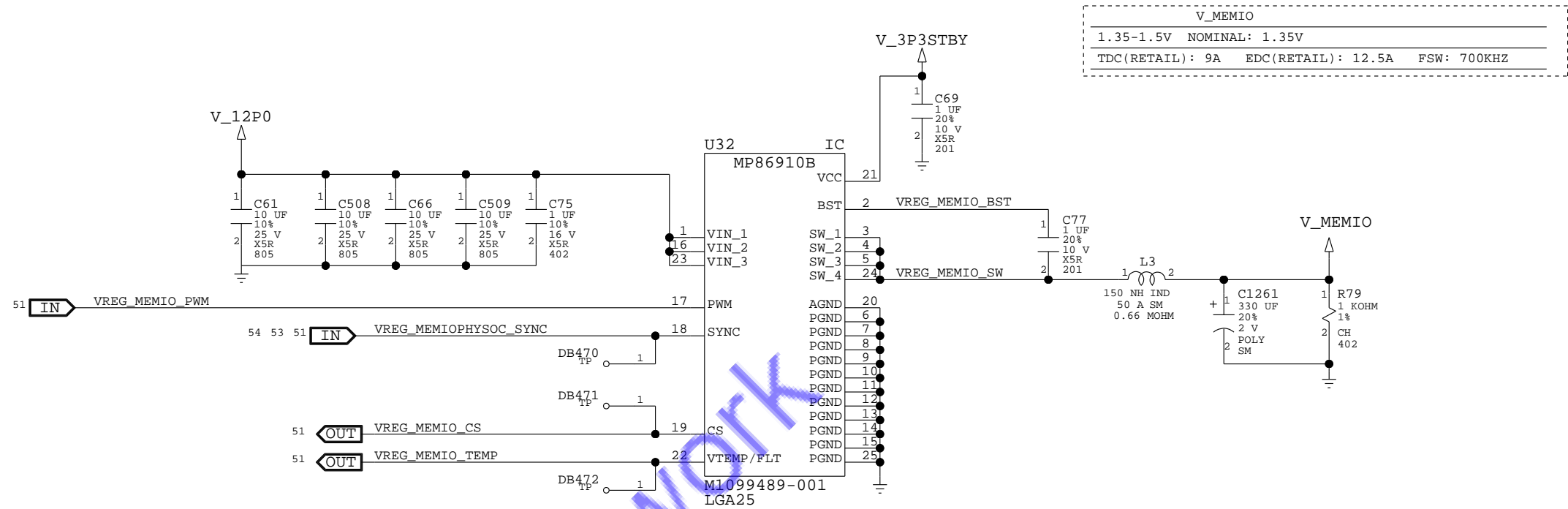
MP2926 RAIL ASSIGNMENTS		
RAIL 1:	V_MEMPHY	(POWER GROUP B)
RAIL 2:	V_MEMIO	(POWER GROUP A)
RAIL 3:	V_SOC	(POWER GROUP B)

MP2926 I2C ADDRESS				
	7-BIT BASE	R/W	I2C ADDR	8-BIT HEX
WRITE	010 0001	0	0X23	0X46
READ	010 0001	1	0X23	0X47

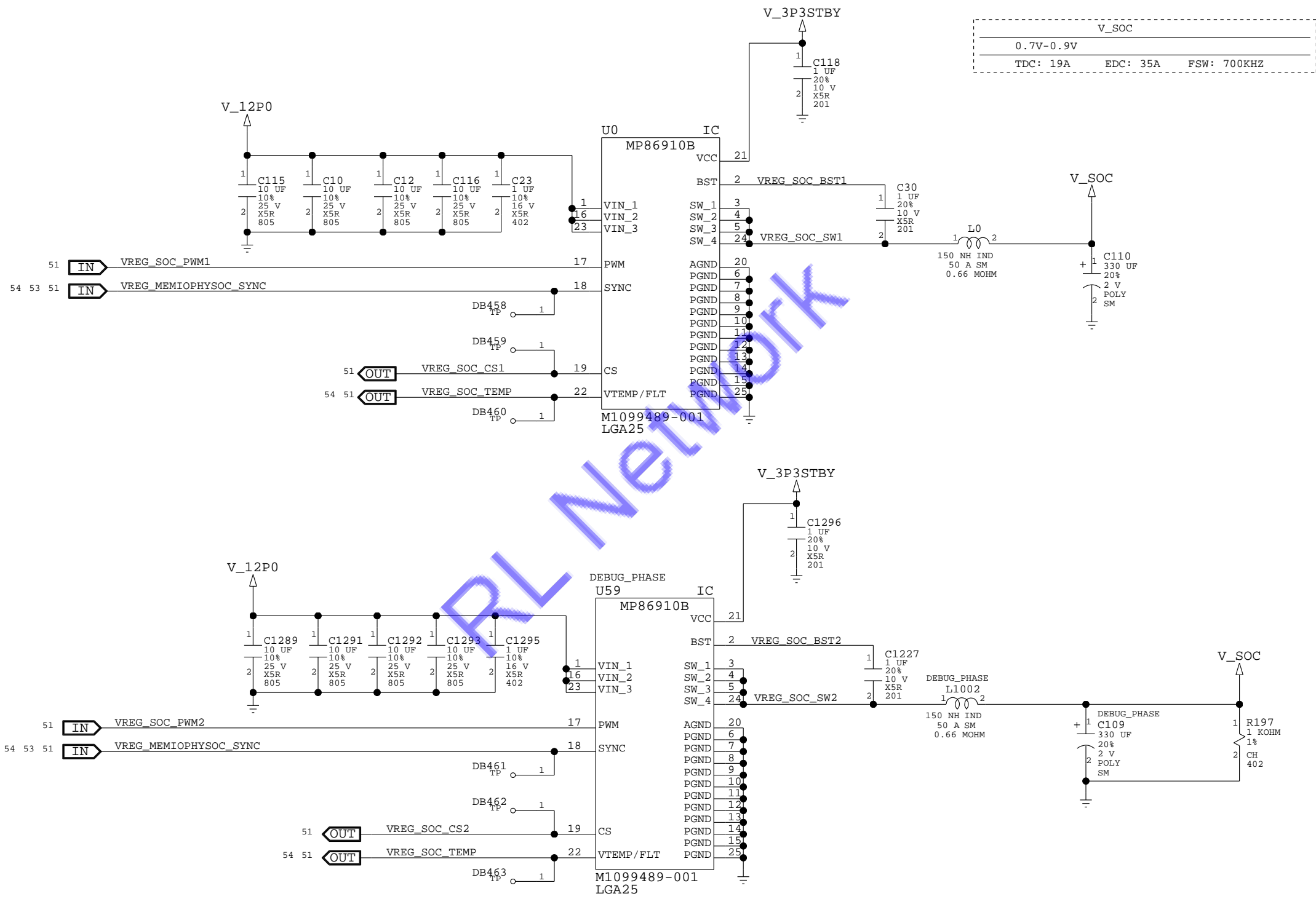
MP2926 RAIL ASSIGNMENTS		
RAIL 1:	V_MEMPHY	(POWER GROUP B)
RAIL 2:	V_MEMIO	(POWER GROUP A)
RAIL 3:	V_SOC	(POWER GROUP B)



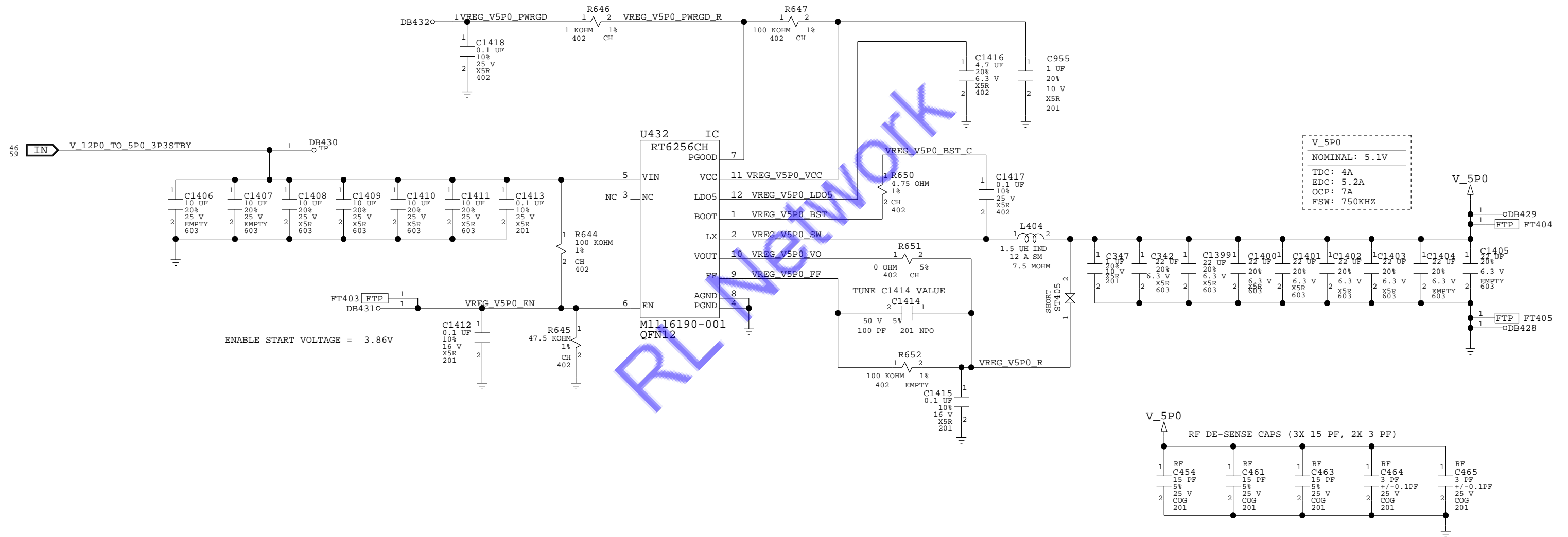
VREGS: V\_MEMIO AND V\_MEMPHY OUTPUT



VREGS: V\_SOC OUTPUT



```
VREGS:  V_5P0
```



MICROSOFT CONFIDENTIAL	PROJECT NAME Stockton	PAGE 55/76	CSA PAGE 55/76	FAB C	VER 0.12
---------------------------	--------------------------	---------------	----------------------	----------	-------------

VREGS: V\_SOC1P8, V\_DRAM1P8

D

C

B

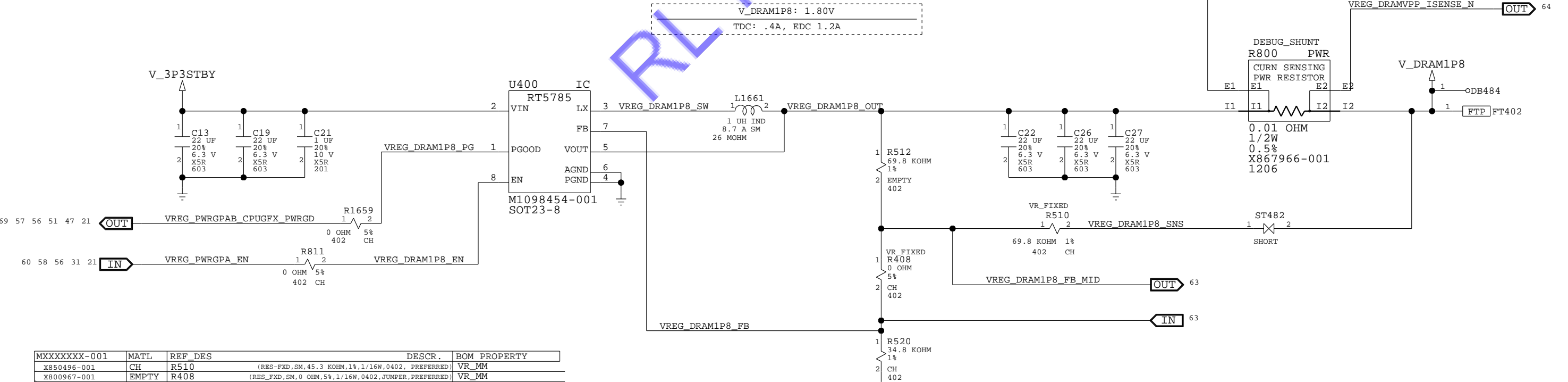
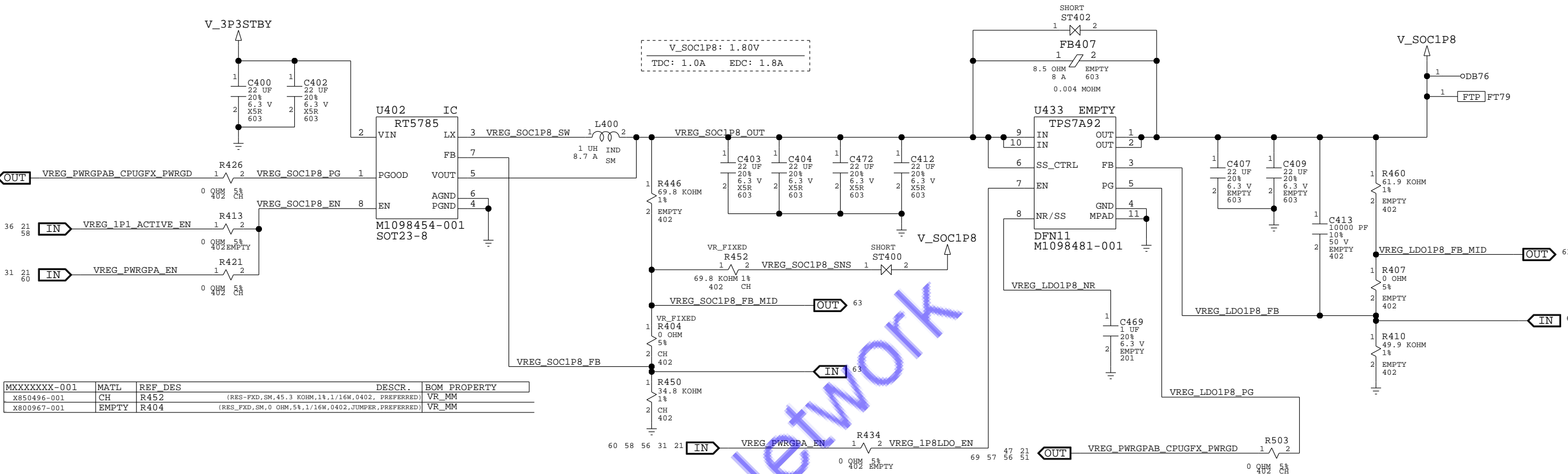
A

D

C

B

A



VREGS: V\_SOCPHY, V\_FUSE

D

D

C

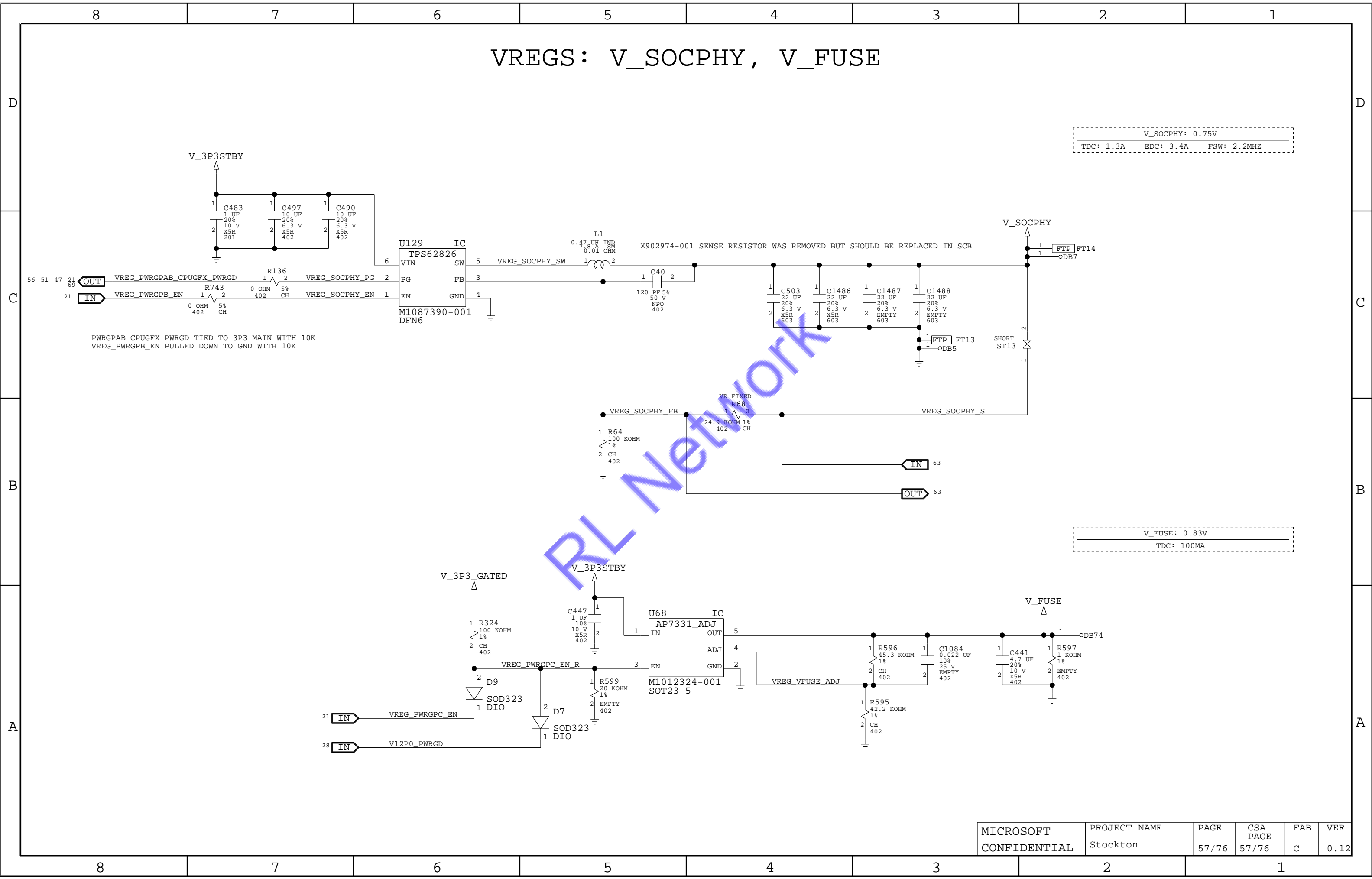
C

B

B

A

A

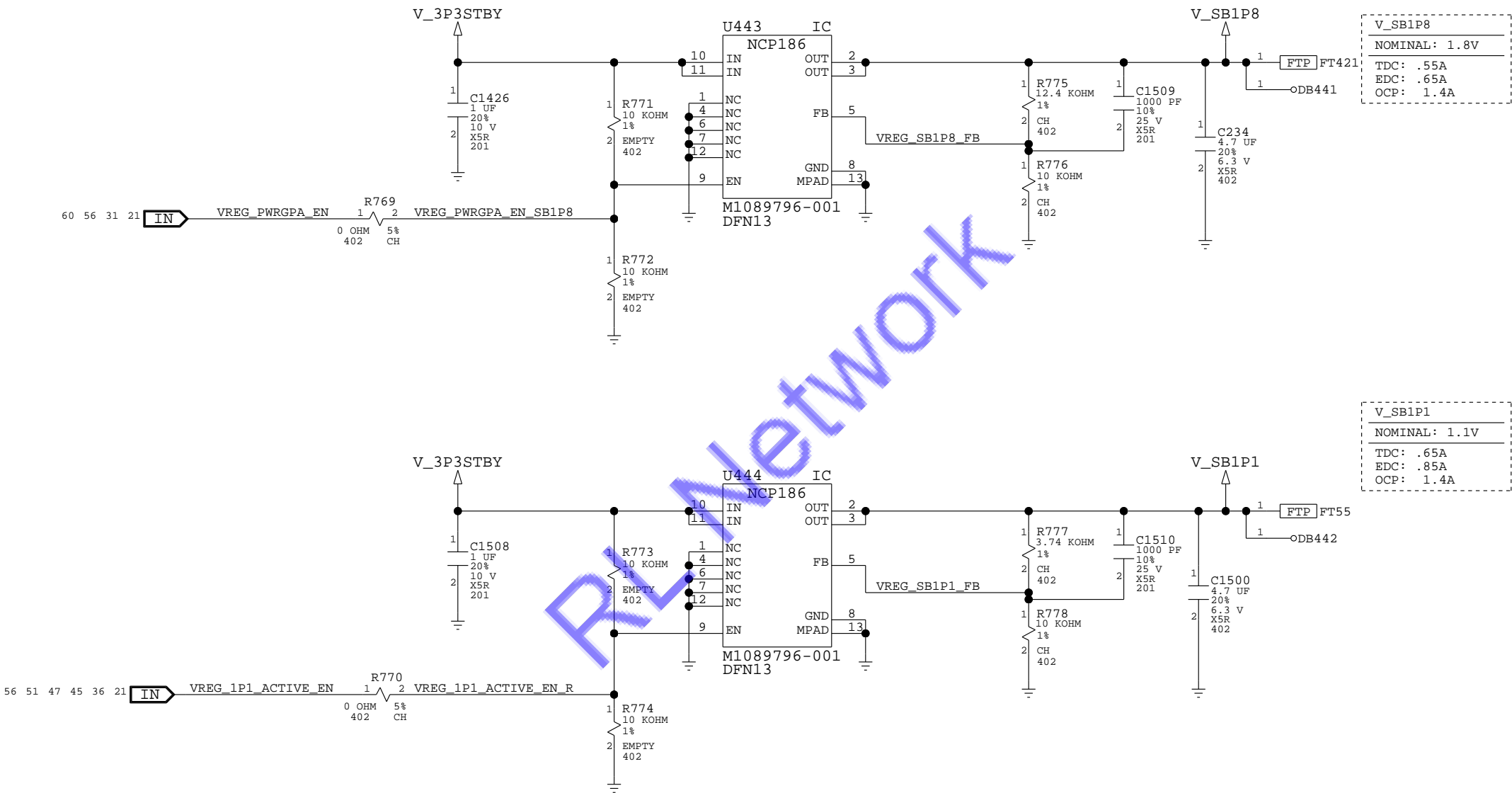


V\_SOCPHY: 0.75V  
TDC: 1.3A EDC: 3.4A FSW: 2.2MHZ

V\_FUSE: 0.83V  
TDC: 100MA

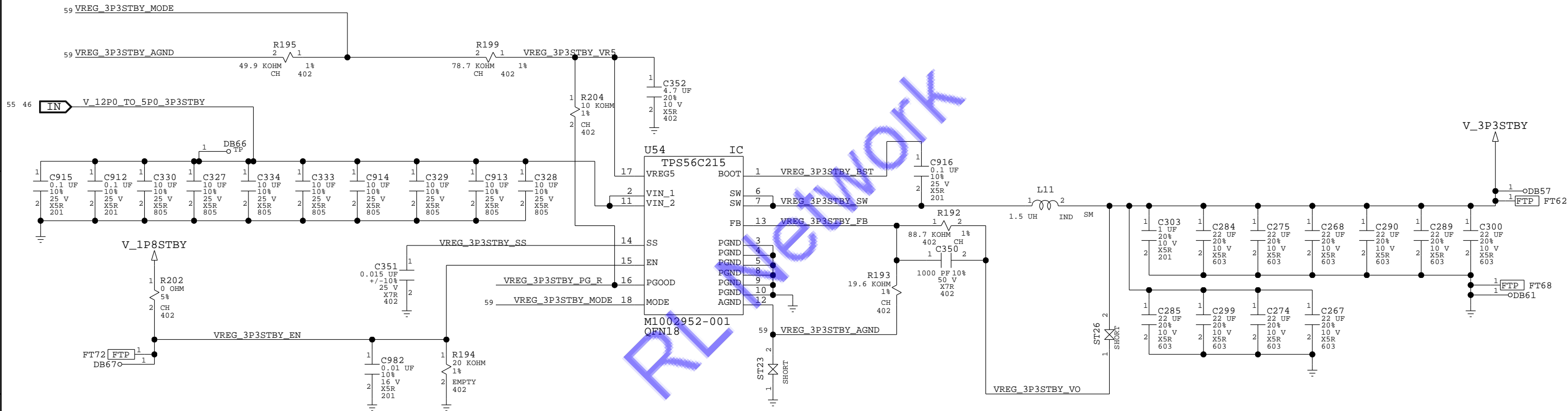


VREGS: V\_SB1P8, V\_SB1P1



VREGS: V\_3P3STBY

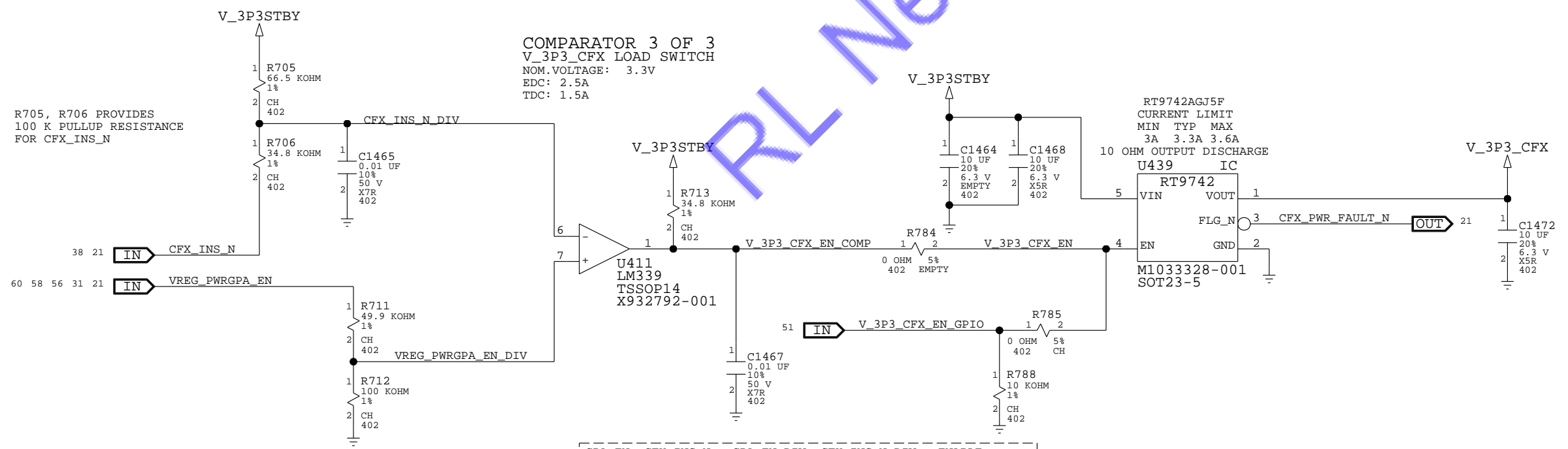
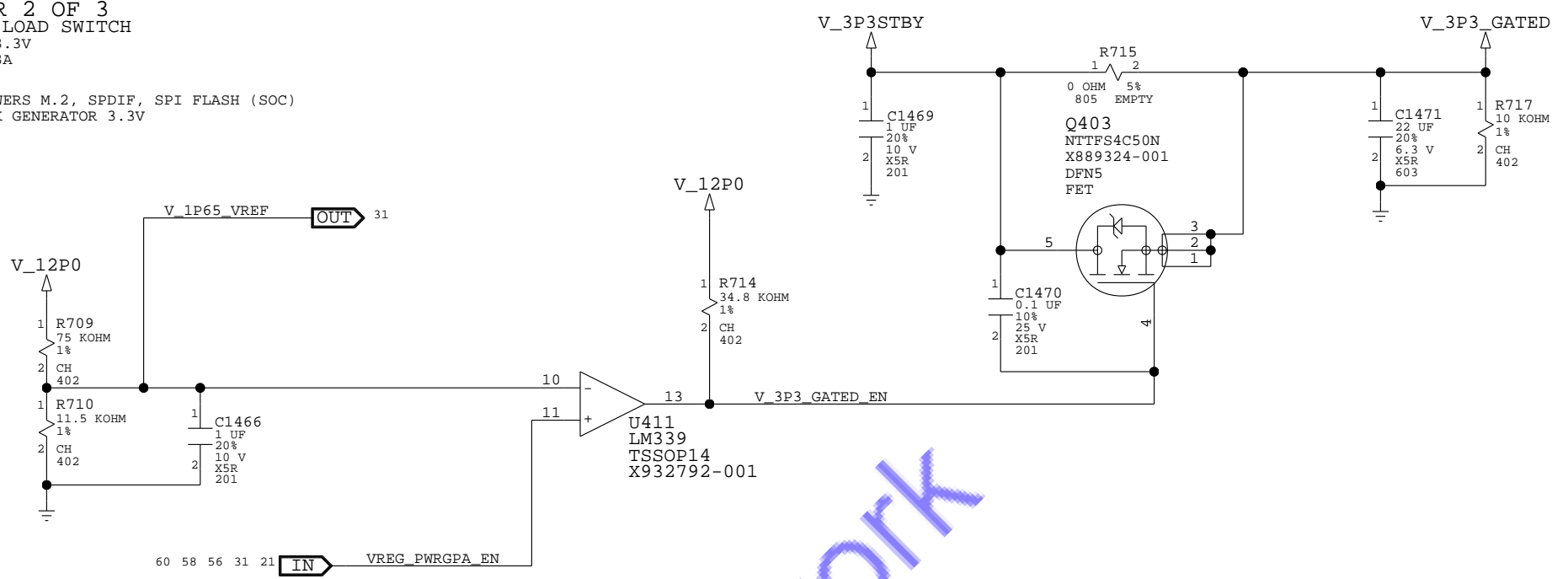
V\_3P3STBY  
NOM. VOLTAGE: 3.32  
EST TDC = 9A  
EST EDC = 12A



VREGS: V\_3P3\_GATED, V\_3P3\_CFX

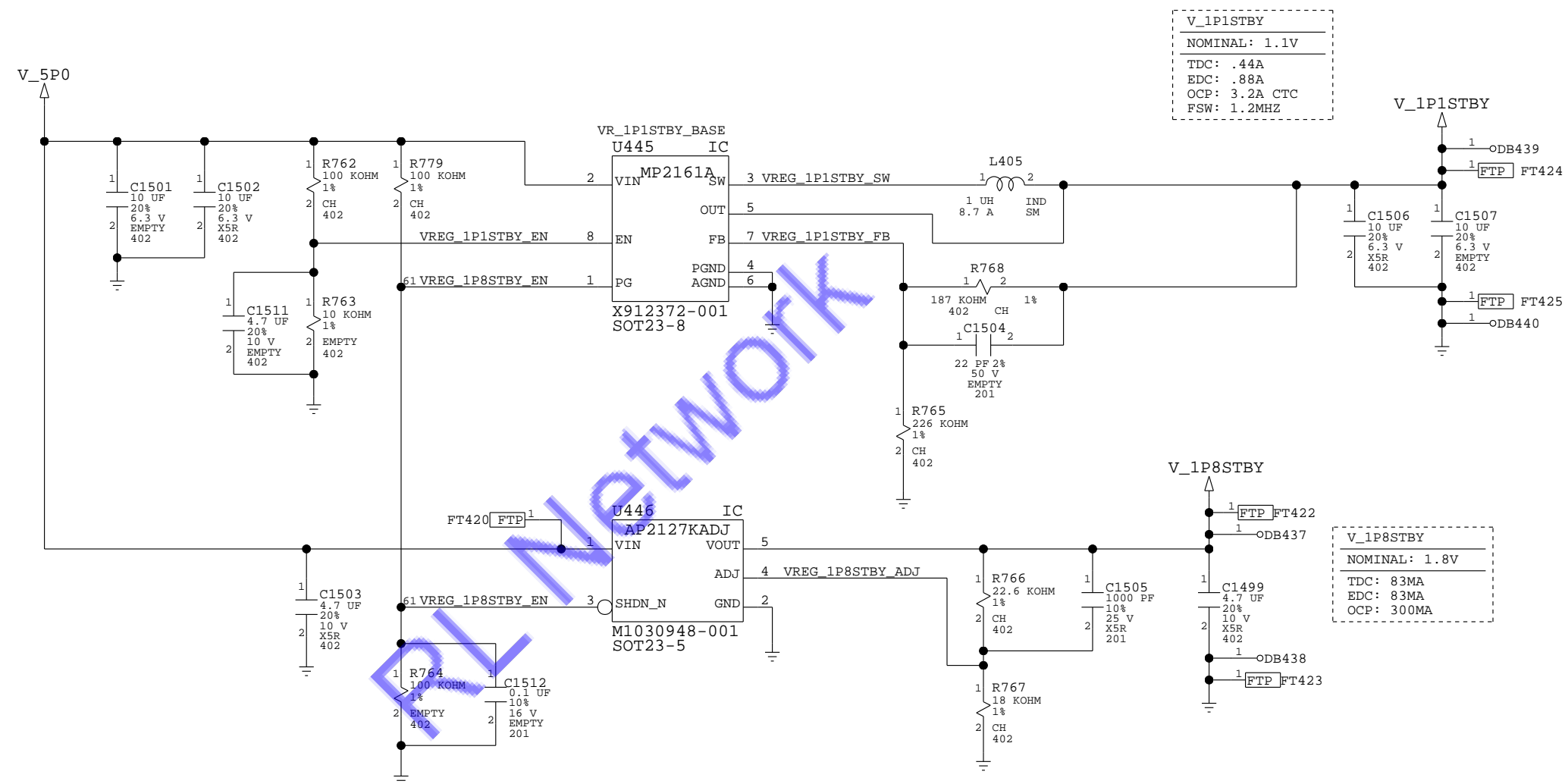
COMPARATOR 2 OF 3  
V\_3P3\_GATED LOAD SWITCH  
NOM.VOLTAGE: 3.3V  
PEAK CURRENT: 3A

V\_3P3\_GATED POWERS M.2, SPDIF, SPI FLASH (SOC)  
SOC VDD3, CLOCK GENERATOR 3.3V



GPA_EN	CFX_INS_N	GPA_EN_DIV	CFX_INS_N_DIV	ENABLE
3.3V	0V	2.2V	1.13V	3.3V
3.3V	3.3V	2.2V	3.3V	0V
0V	0V	0V	1.13V	0V
0V	3.3V	0V	3.3V	0V

VREGS: V\_1P1STBY, V\_1P8STBY

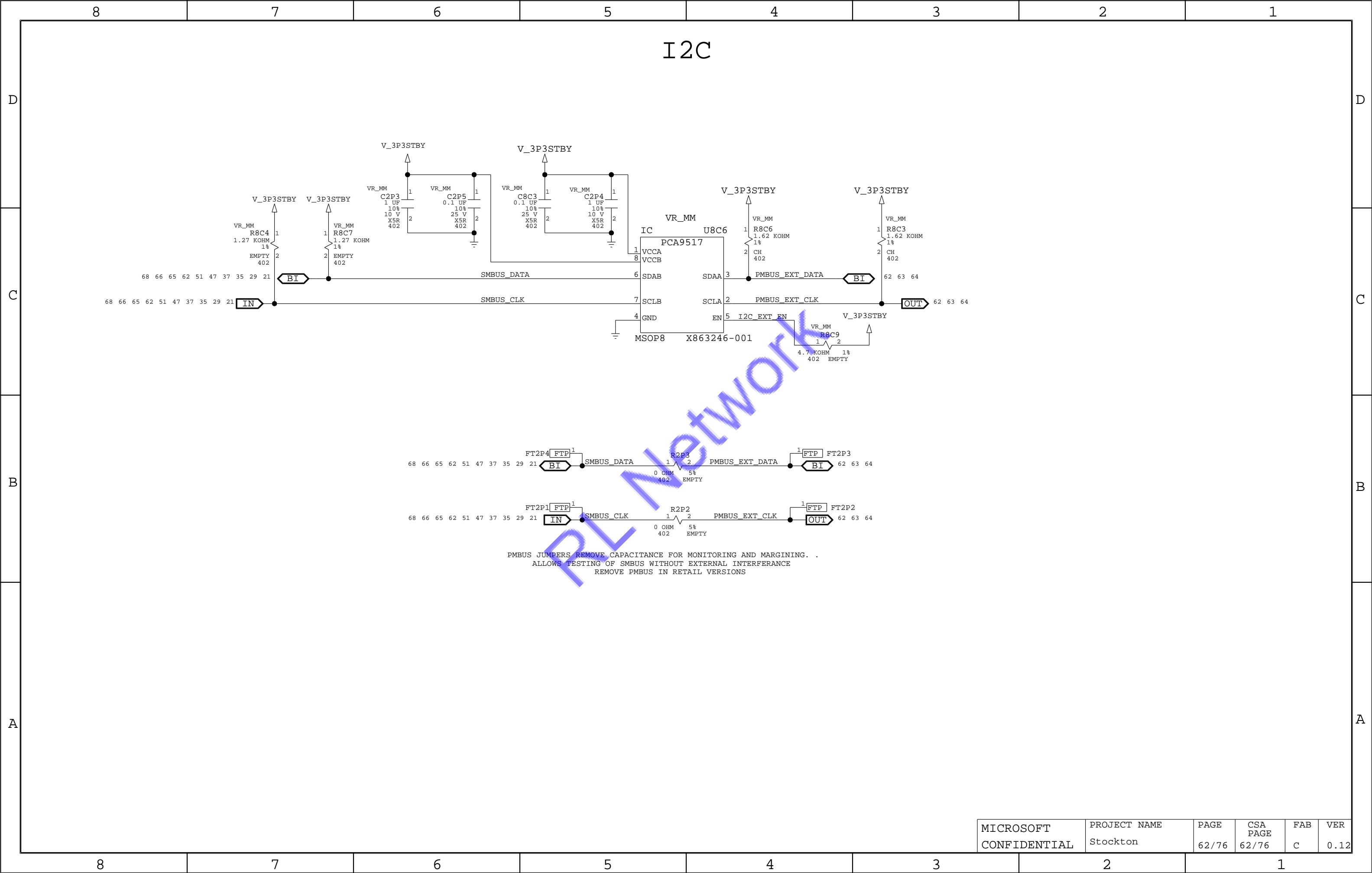


V_1P1STBY
NOMINAL: 1.1V
TDC: .44A
EDC: .88A
OCF: 3.2A CTC
FSW: 1.2MHZ

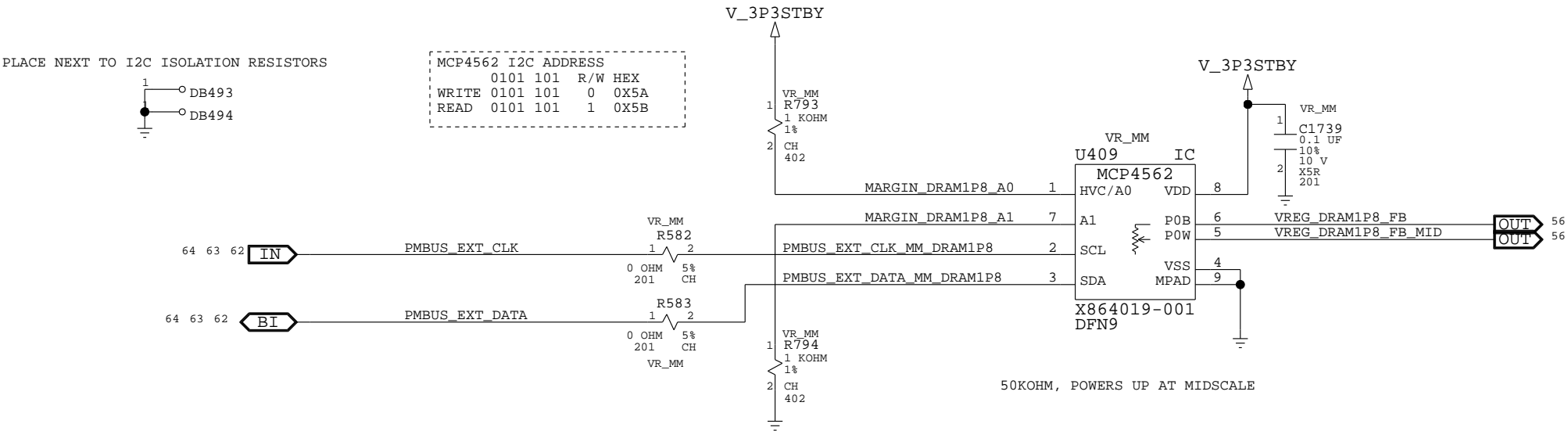
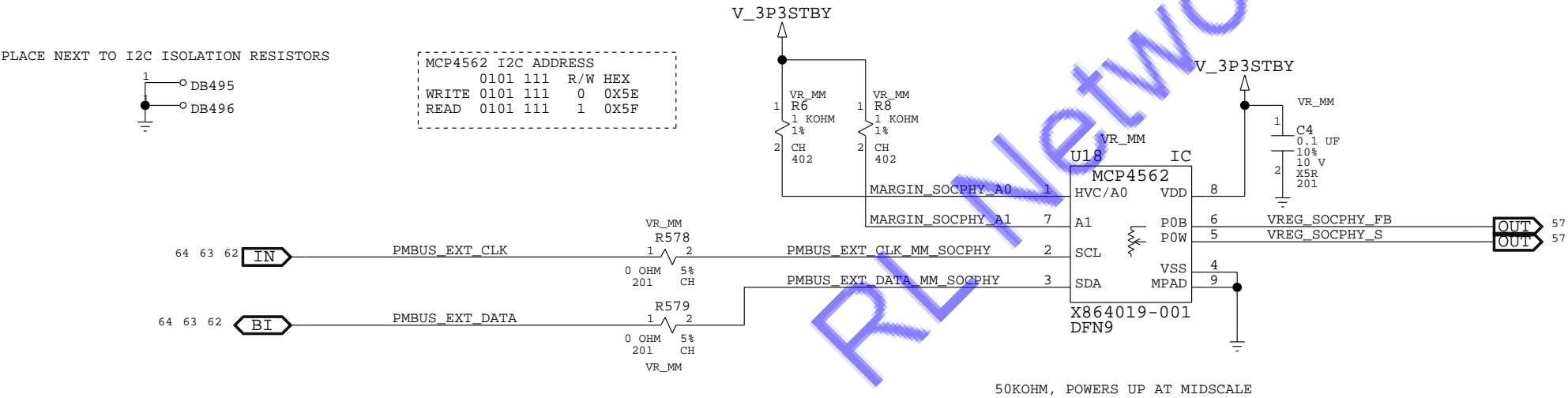
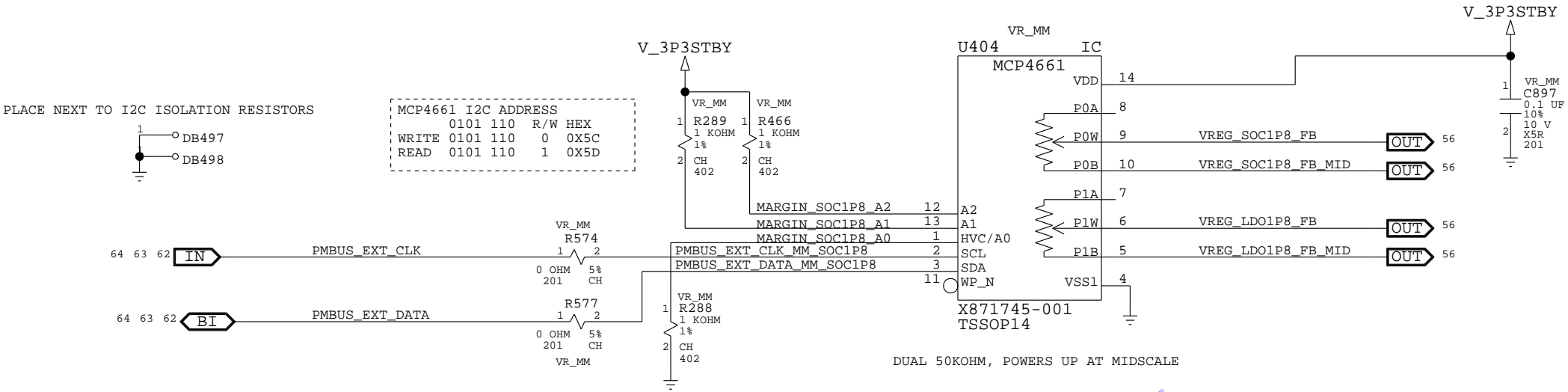
V_1P8STBY
NOMINAL: 1.8V
TDC: 83MA
EDC: 83MA
OCF: 300MA

MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM_PROPERTY
X912372-001	IC	U445	IC-PWR,VREG,SM,TSOT23-8,STEP DOWN,6V,2A,MP2161A	VR_1P1STBY_MPS
M1018565-001	IC	U445	IC-PWR,VREG,SM,TSOT23-8,STEP DOWN,6V,2A,RICHTER,RT5785C QUAL	VR_1P1STBY_RT

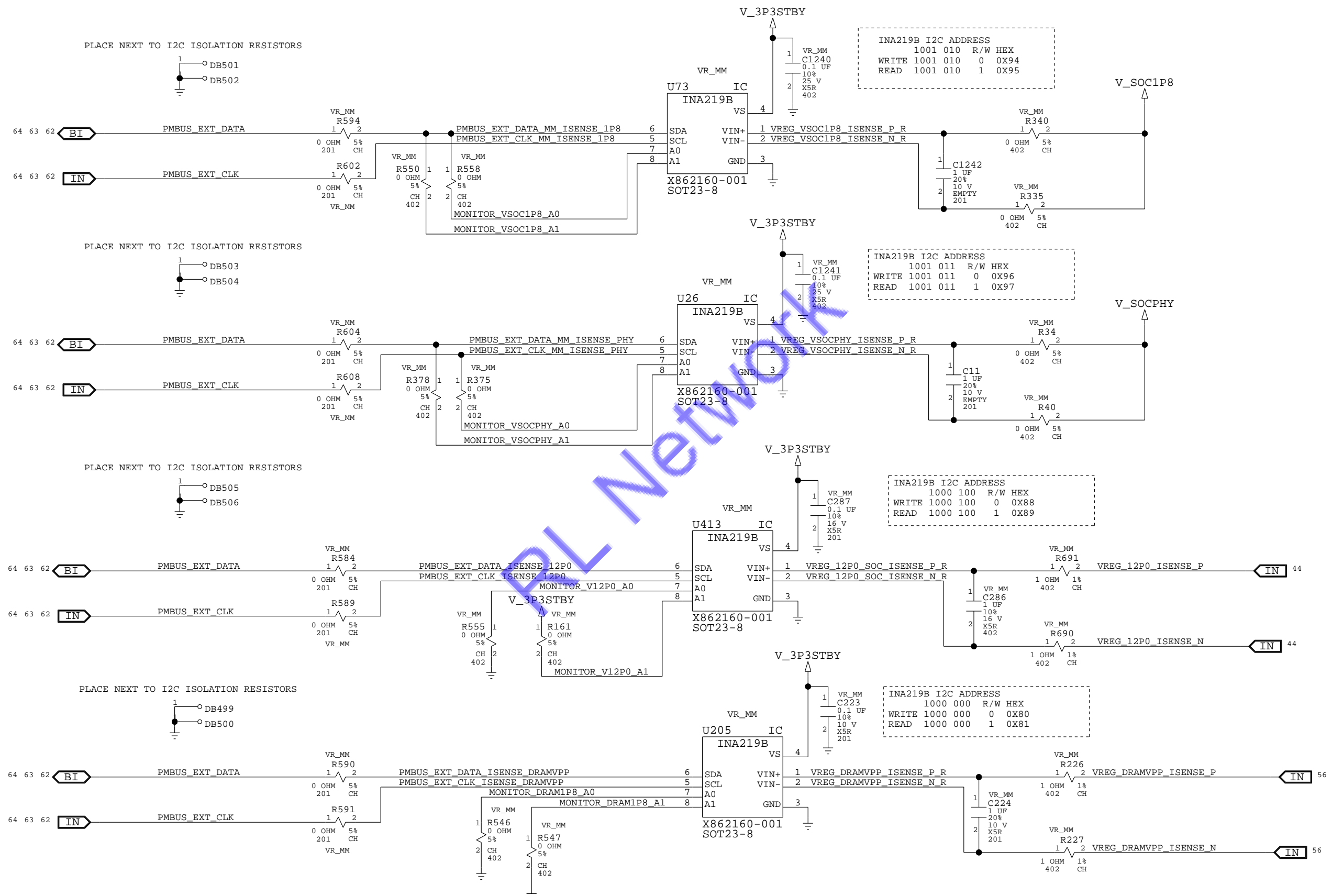
MICROSOFT CONFIDENTIAL	PROJECT NAME Stockton	PAGE 61/76	CSA PAGE 61/76	FAB C	VER 0.12
---------------------------	--------------------------	---------------	----------------------	----------	-------------



DEBUG: MARGIN V\_SOCPHY,V\_SOC1P8, V\_DRAM1P8

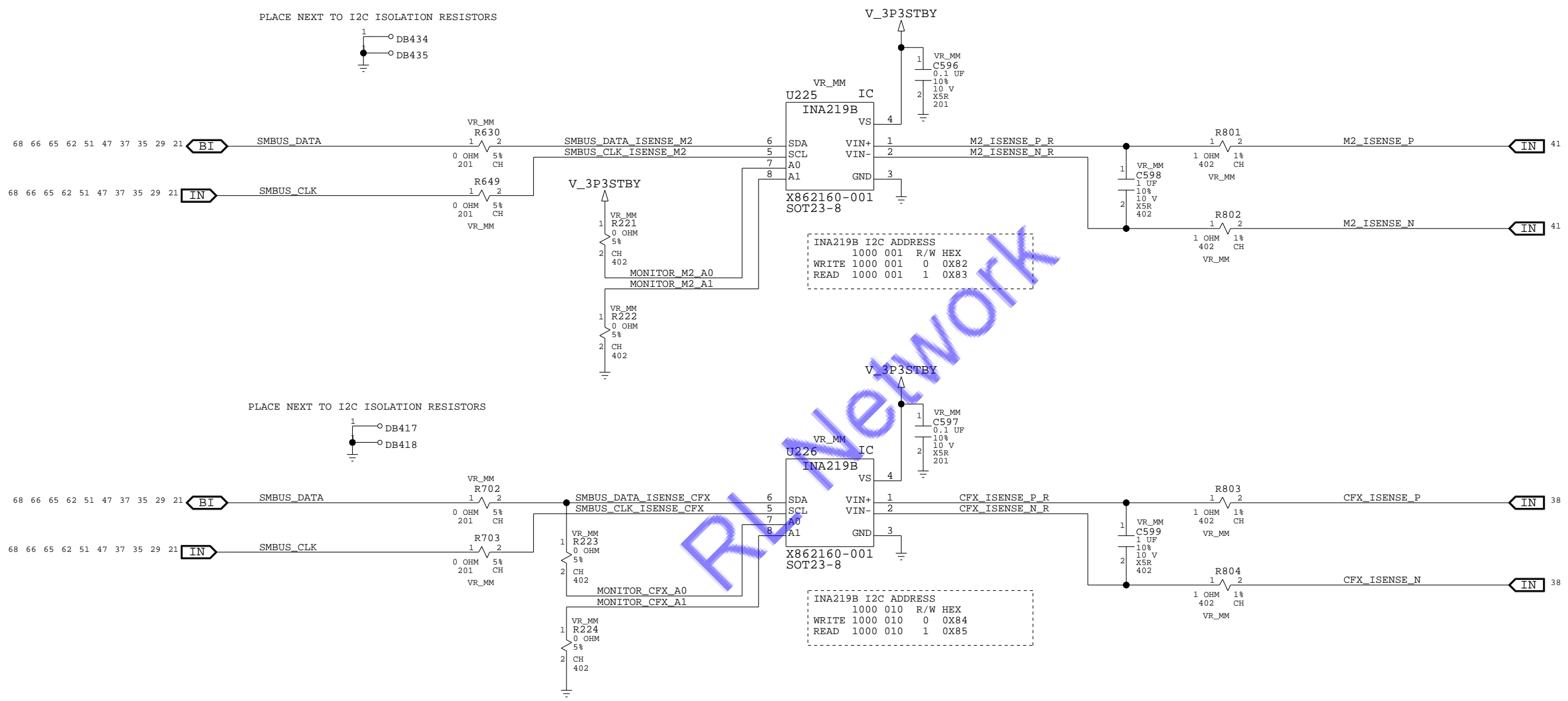


```
DEBUG: MONITOR V_SOC1P8, V_SOCPHY, V_12P0, V_DRAM1P8
```

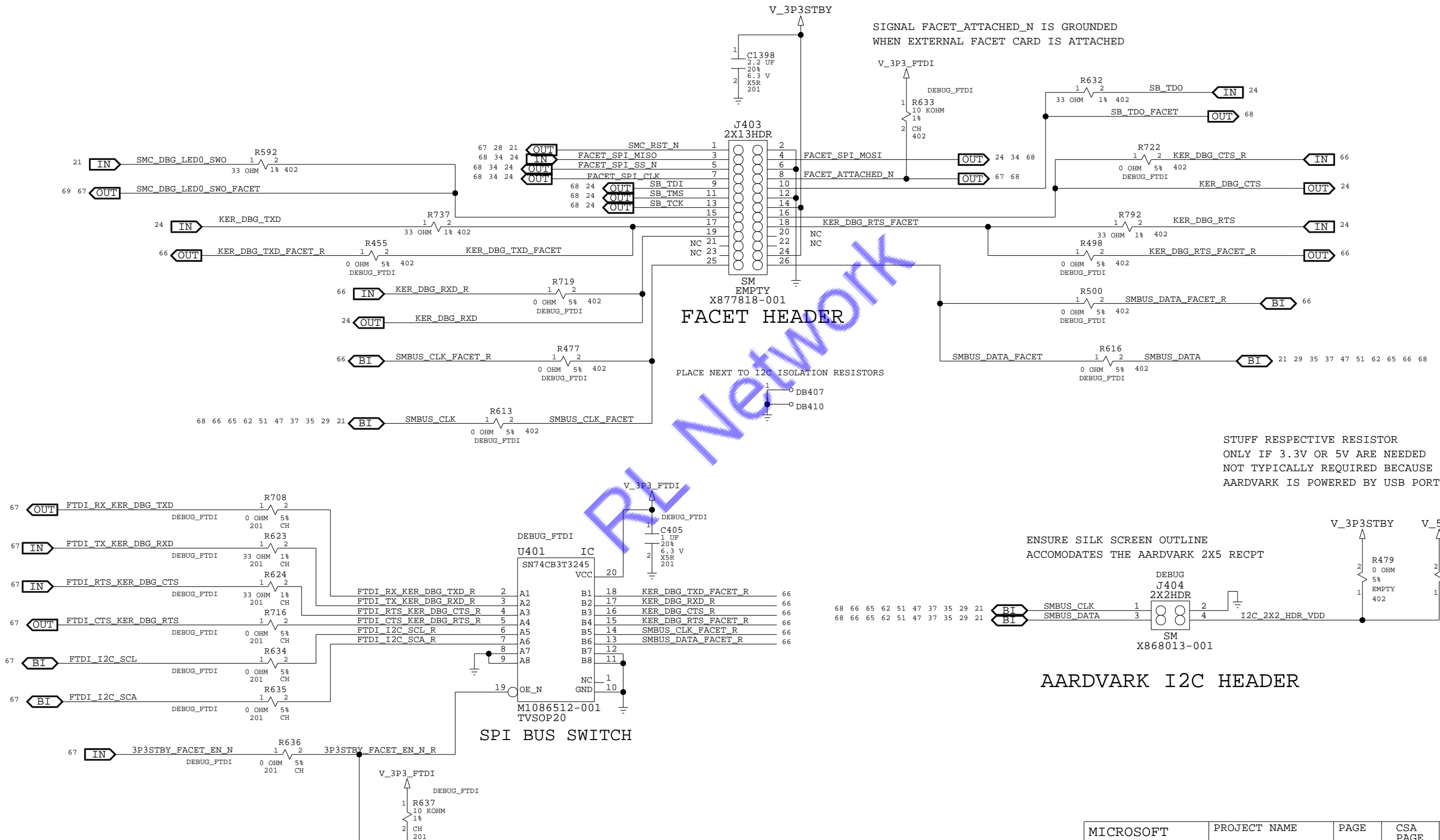




DEBUG: MONITOR M.2. CFEXPRESS

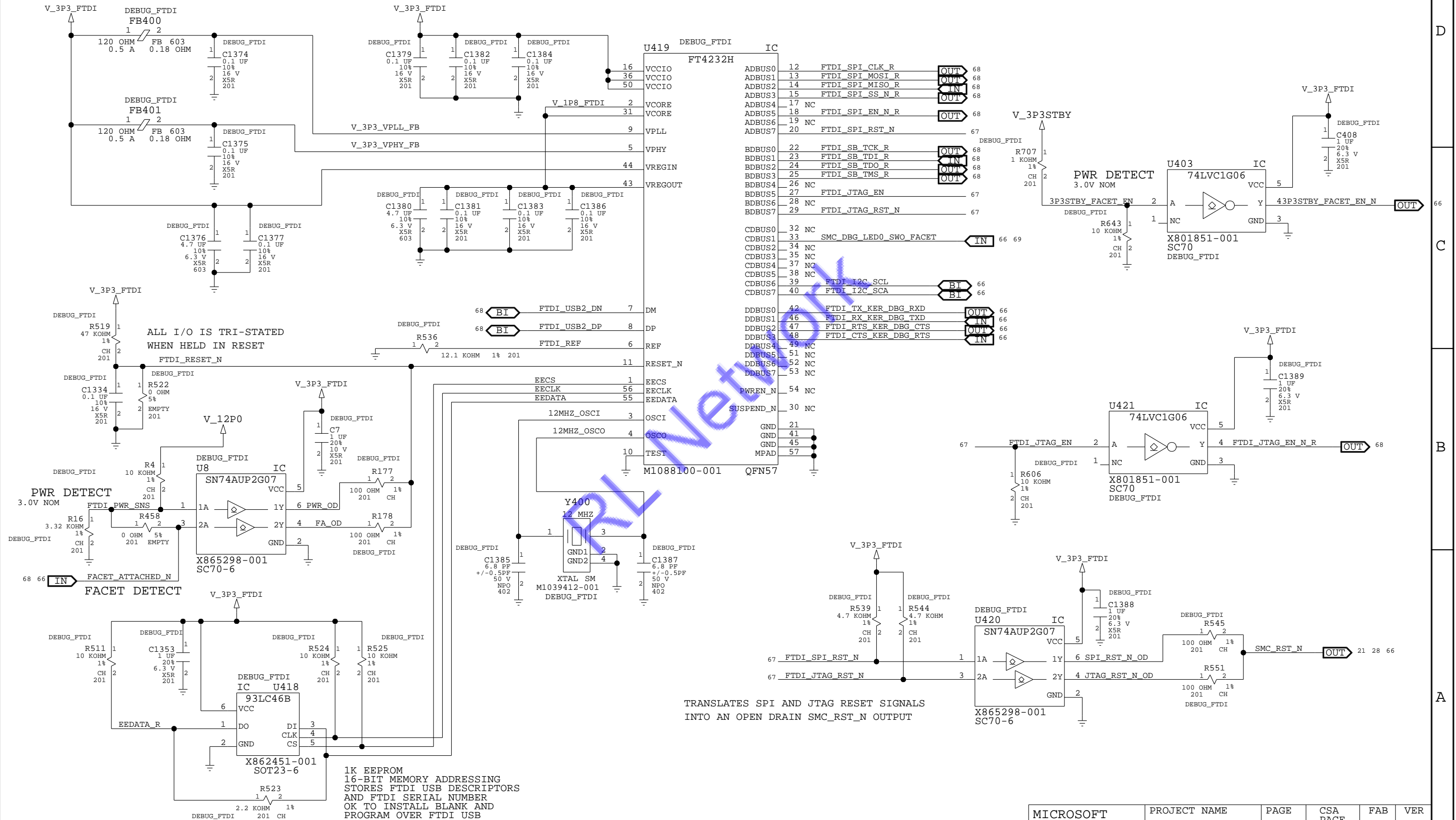


DEBUG: FACET HEADER

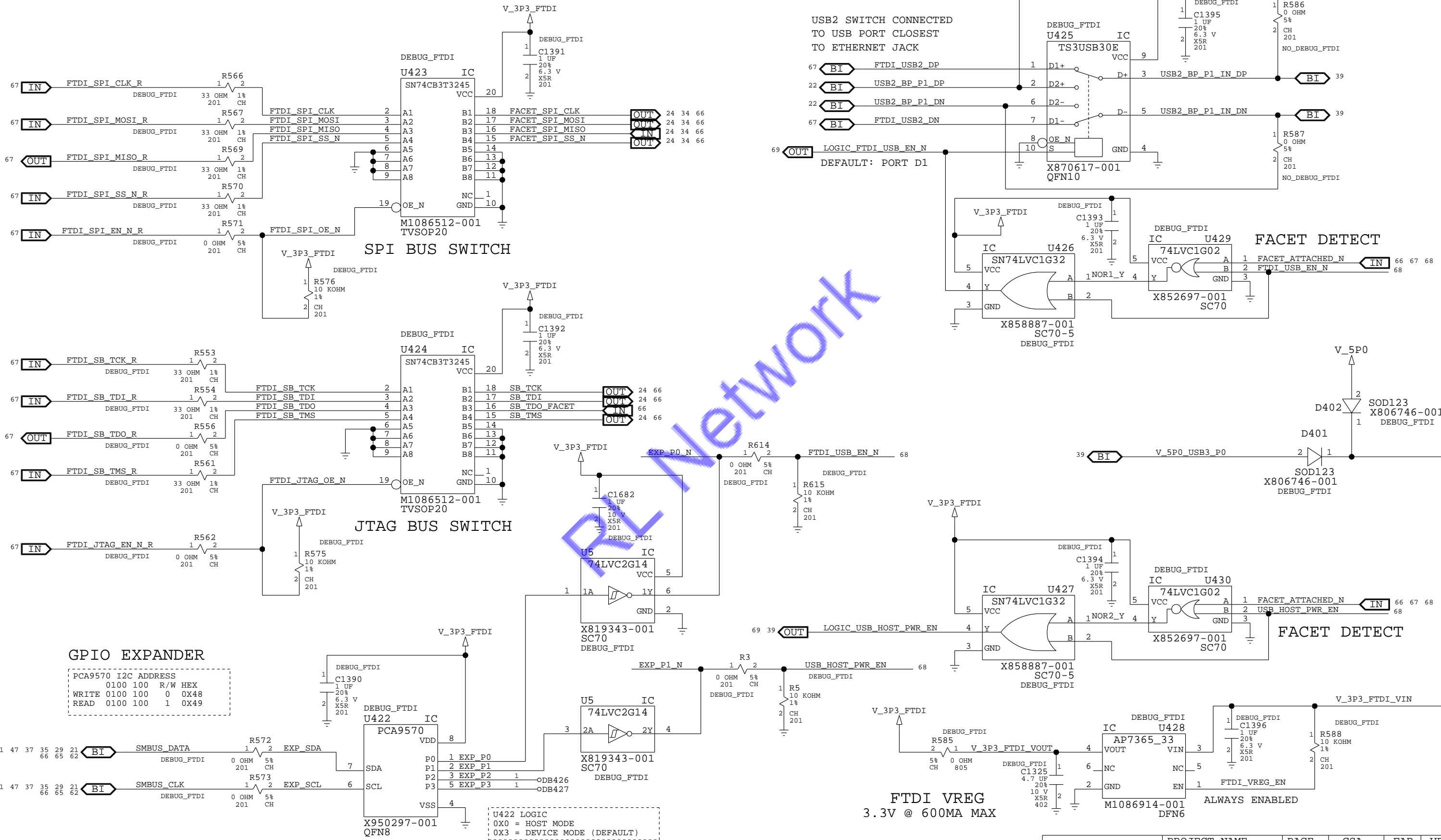


MICROSOFT CONFIDENTIAL	PROJECT NAME Stockton	PAGE 66/76	CSA PAGE 66/76	FAB C	VER 0.12
---------------------------	--------------------------	---------------	----------------------	----------	-------------

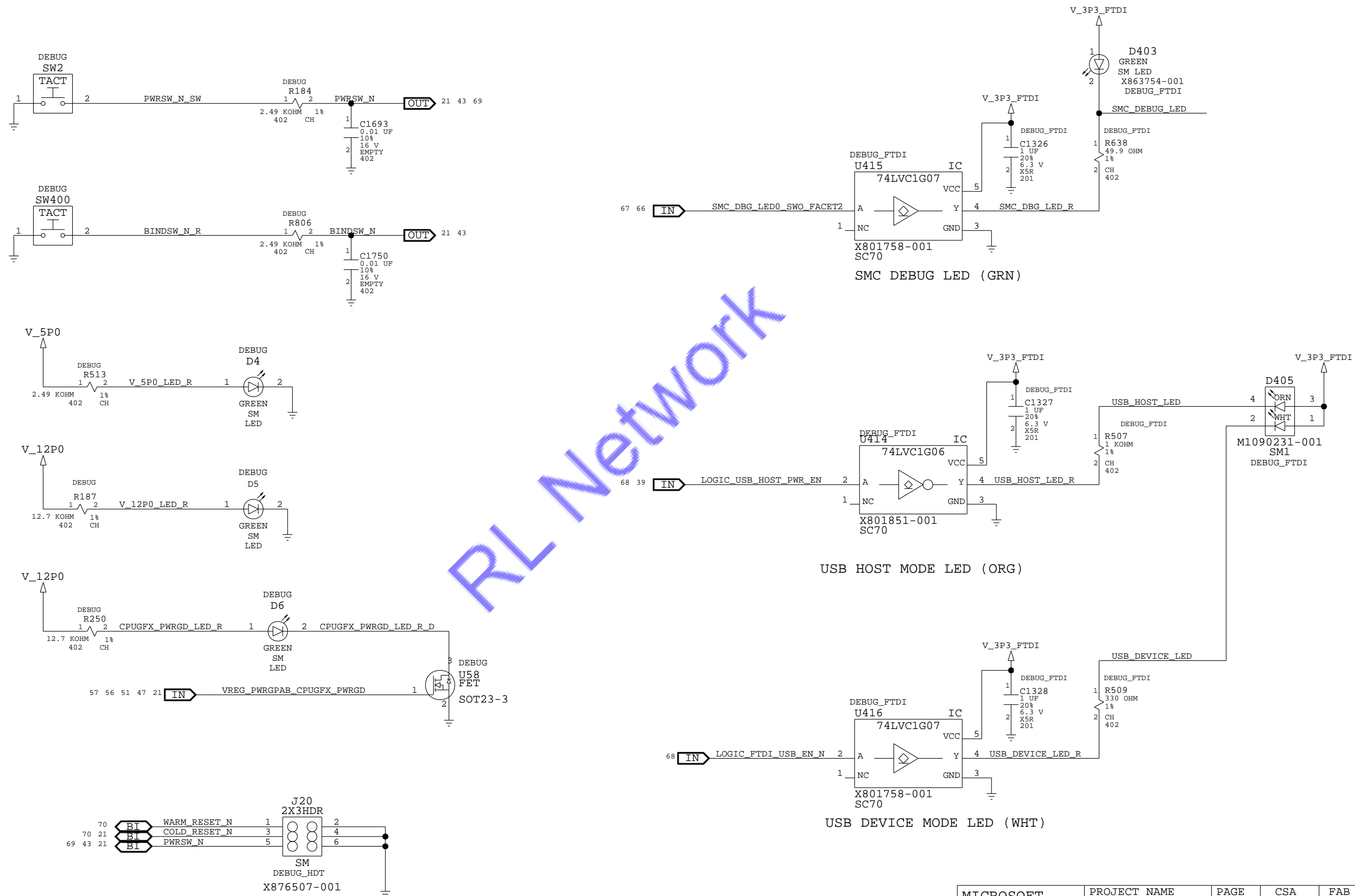
DEBUG: FTDI BRIDGE



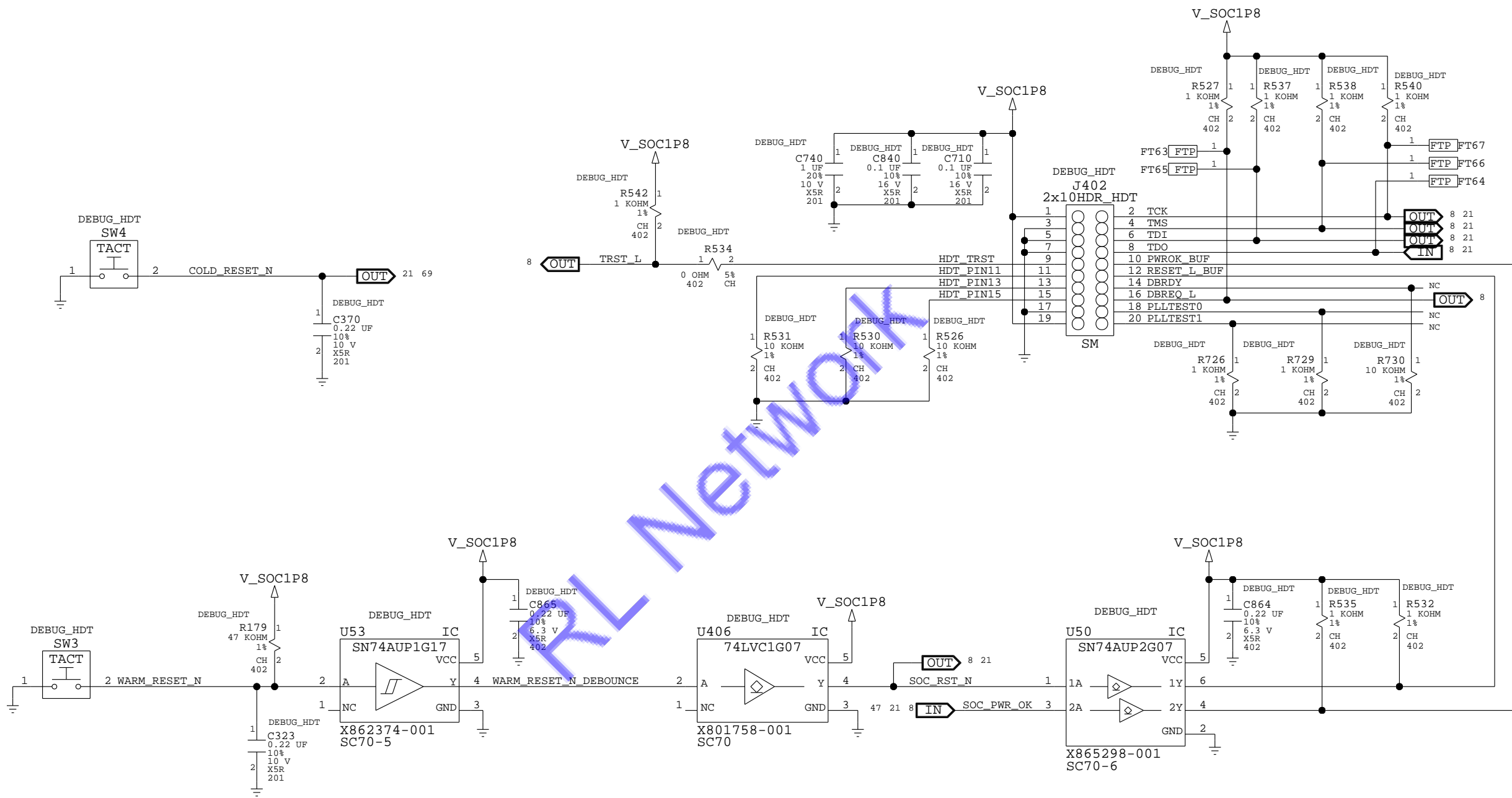
# DEBUG: FTDI BUFF, USB, PWR



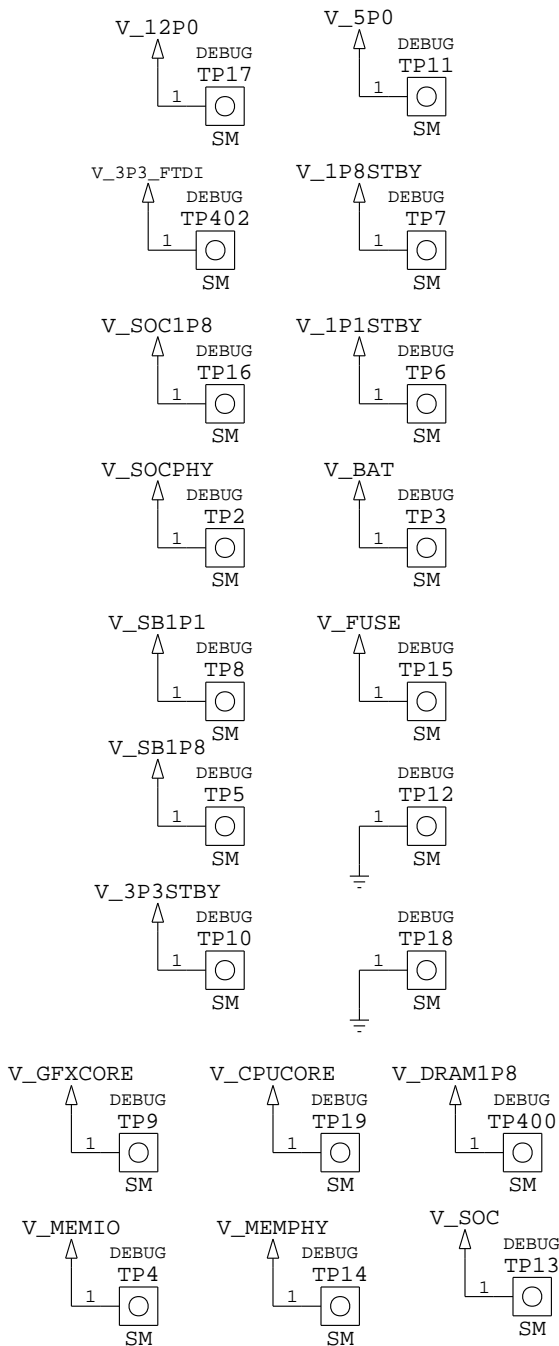
DEBUG: SWITCHES, LEDS



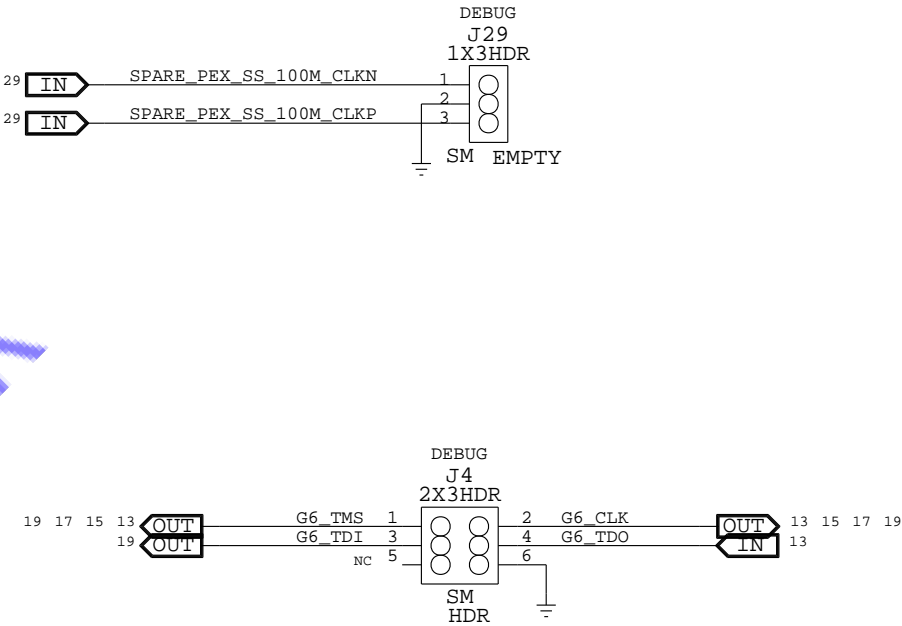
DEBUG: HDT



DEBUG: VR HEADERS, TEST POINTS, CONNECTORS



PCIE CONNECTORS

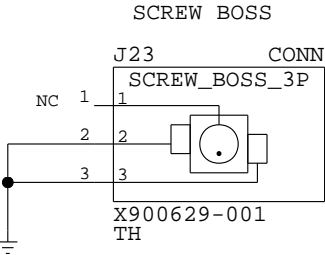
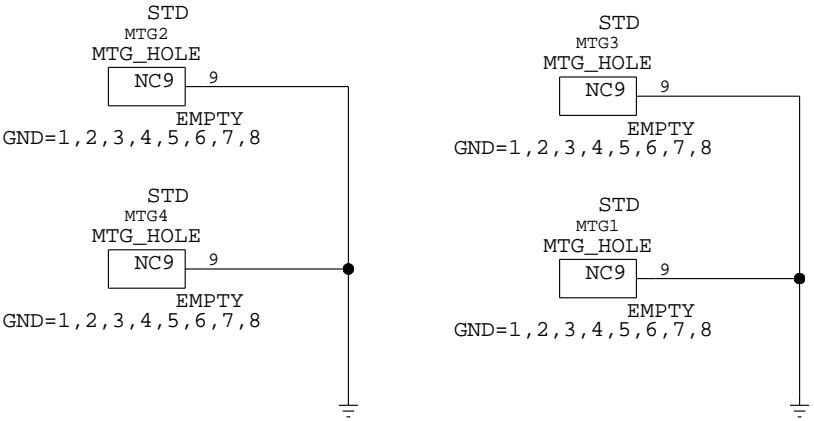


NOTE: THESE TEST POINTS ARE NOT  
TO BE USED FOR VOLTAGE REGULATOR  
QUALIFICATION TEST POINTS

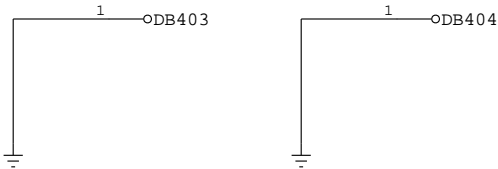


LABELS AND MOUNTING

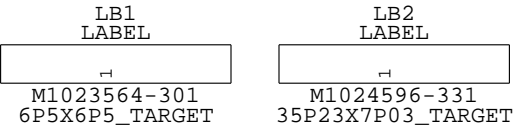
HEAT SINK MOUNTING HOLES



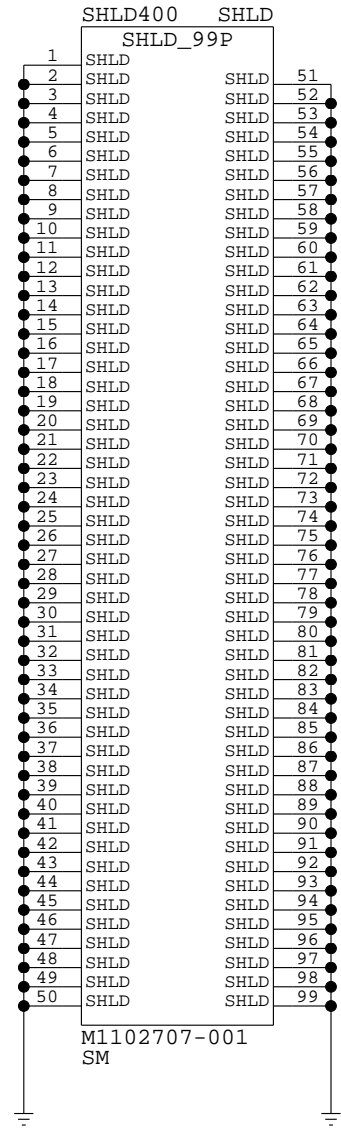
GND PADS FOR HEATSINK ALIGNMENT PINS



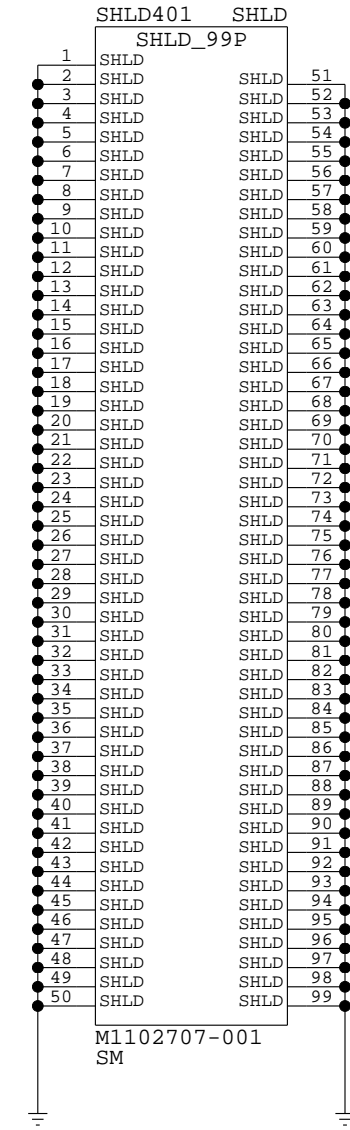
INTELLIGENT SERIAL NUMBER TARGET



TOP BOARD LEVEL SHIELD



BOTTOM BOARD LEVEL SHIELD



MXXXXXXX-001	MATL	REF DES	DESCR.	BOM PROPERTY
M1111890-001	FR4	PCB1	PCB, STOCKTON, FAB B, 8 LAYERS, G	PCB_GI
MXXXXXXX-001	FR4	PCB1	PCB, STOCKTON, FAB B, 8 LAYERS, OSP	PCB_OSP

8		7		6		5		4		3		2		1	
BOM DEFINITIONS															
D	BOM		DEFINITION												
	AUDIO		INCLUDES COMPONENTS FOR THE STANDARD AUDIO SOLUTION												
	AUDIO_PREM		INCLUDES COMPONENTS FOR THE PREMIUM SE/LE SPEAKER SOLUTION												
	COMMON		ALL COMPONENTS WITH NO BOM PROPERTY												
C	DEBUG		COMPONENTS REQUIRED FOR BRING UP & DEBUG												
	DEBUG_HDT		HDT-RELATED DEBUG COMPONENTS												
	DEBUG_SHUNT		COMPONENTS WHICH ARE ON DEBUG BOARDS, BUT ARE REMOVED/SHORTED ON RETAIL												
	EMMC_BASE		DUMMY PLACE HOLDER FOR EMMC DEVICE & RESISTORS. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_16NM, EMMC TOSHIBA_15NM, EMMC SAMSUNG_14NM												
	EMMC_HYNIX_16NM		HYNIX EMMC DEVICE												
	EMMC_SAMSUNG_14NM		SAMSUNG EMMC DEVICE												
	EMMC_TOSHIBA_15NM		TOSHIBA EMMC DEVICE												
	SANTO_BASE		DUMMY PLACE HOLDER FOR SANTO SB. NEVER USE THIS IN THE RECIPE FILE. USE ONE OF THESE INSTEAD: SANTO_DEV OR SANTO_RETAIL												
	SANTO_DEV		DEBUG VERSION OF SANTO SB												
	SANTO_RETAIL		RETAIL VERSION OF SANTO SB												
	M2_ONLY		POPULATE TO SUPPORT AN M.2 INTERFACE												
	NO_M2		POPULATE WHEN THERE IS NO M2. INTERFACE												
B	PCB_GI		FAB TYPE: GOLD												
	PCB_OSP		FAB TYPE: ORGANIC SOLDERABILITY PRESERVATIVE GREEN SOLDERMASK												
	PCB_OSP_BLACK		FAB TYPE: ORGANIC SOLDERABILITY PRESERVATIVE BLACK SOLDERMASK												
	RTC_RETAIL		RTC CIRCUIT IMPLEMENTATION FOR RETAIL BOARDS												
	RTC_XDK		RTC CIRCUIT IMPLEMENTATION FOR XDK BOARDS												
	SOC_BASE		DUMMY PLACE HOLDER FOR SOC. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_16NM, EMMC TOSHIBA_15NM, EMMC SAMSUNG_14NM												
	SOC_EMPTY		DOES NOT STUFF SPARKMAN												
	SOC_INCLUDE		STUFFS SPARKMAN												
	VR_FIXED		SET ALL VRS TO FIXED VOLTAGES (NON-MARGINED). EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_MM												
	VR_MM		ALLOWS MOST VRS TO BE MARGINED FOR M&M BOARDS. EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_FIXED												
	RETAIL		COMPONENTS STUFFED FOR A RETAIL CONSOLE. DO NOT USE WITH DEBUG												
	DEBUG_PHASE		PHASES USED FOR INITIAL POWER UP												
A	DRAM_VPP_DEBUG		SEPARATES SOC 1.8V AND DRAM 1.8V. USE IF MARGINING SOC 1.8V OUTSIDE OF DRAM 1.8V LIMITS. NEVER USE WITH DRAM_VPP_RETAIL												
	DRAM_VPP_RETAIL		COMBINES SOC 1,8V AND DRAM1.8V USEING A FILTER NETWORK. NEVER USE WITH DRAM_VPP_DEBUG												
	DEBUG_FTDI		STUFFS INTERCEPT CIRCUITRY FOR DEBUG												
	NO_DEBUG_FTDI		BYPASSES INTERCEPT CIRCUITRY FOR NO DEBUG												
	SPI_FLASH_BASE		DUMMY PLACE HOLDER FOR SPI FLASH. NEVER USE THIS IN THE RECIPE FILE.												
	SPI_FLASH_MACRONIX		STUFFS MACRONIX SPI FLASH												
	SPI_FLASH_WINBOND		STUFFS WINBOND SPI FLASH												
</															

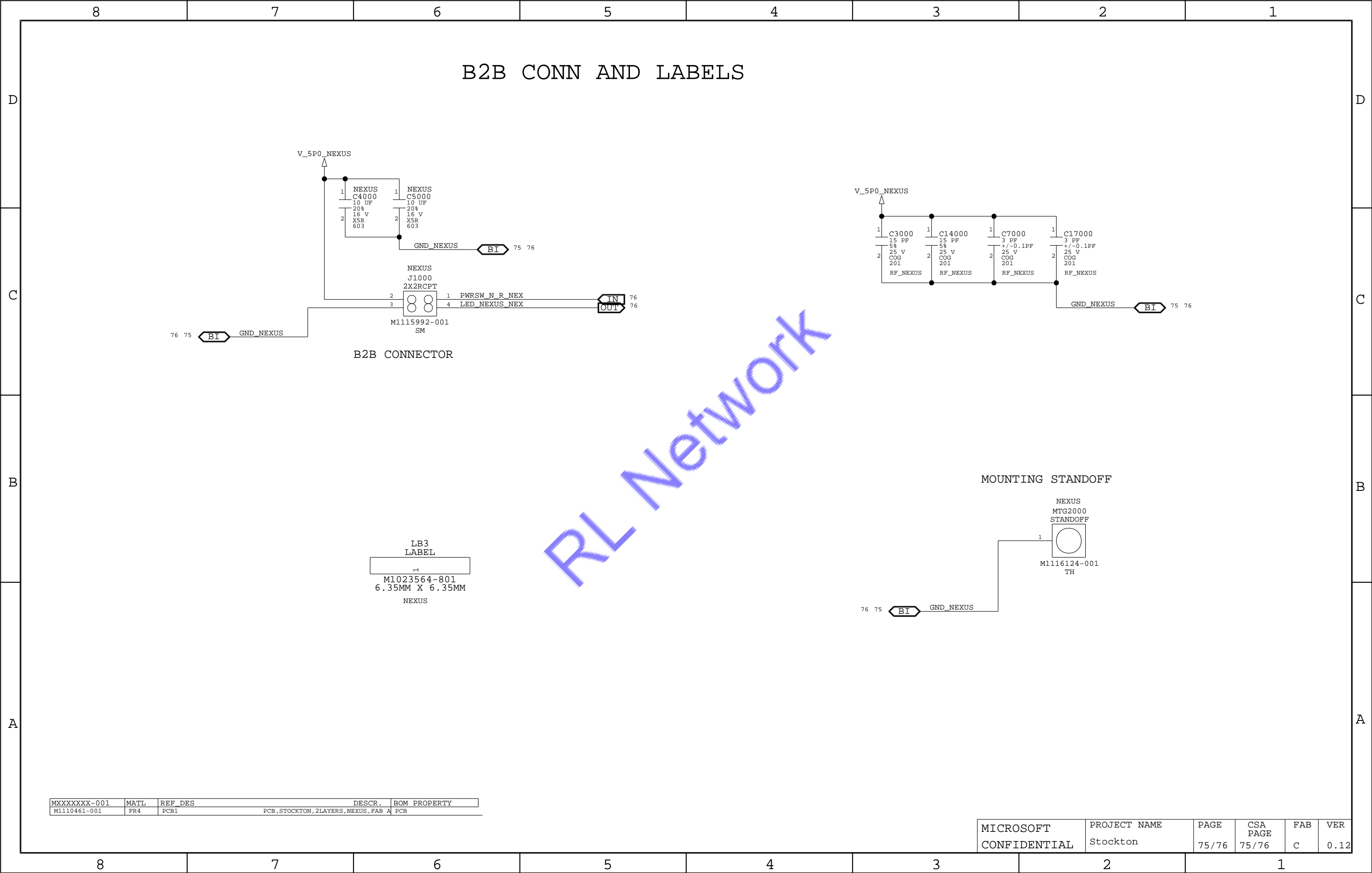
# STOCKTON\_NEXUS

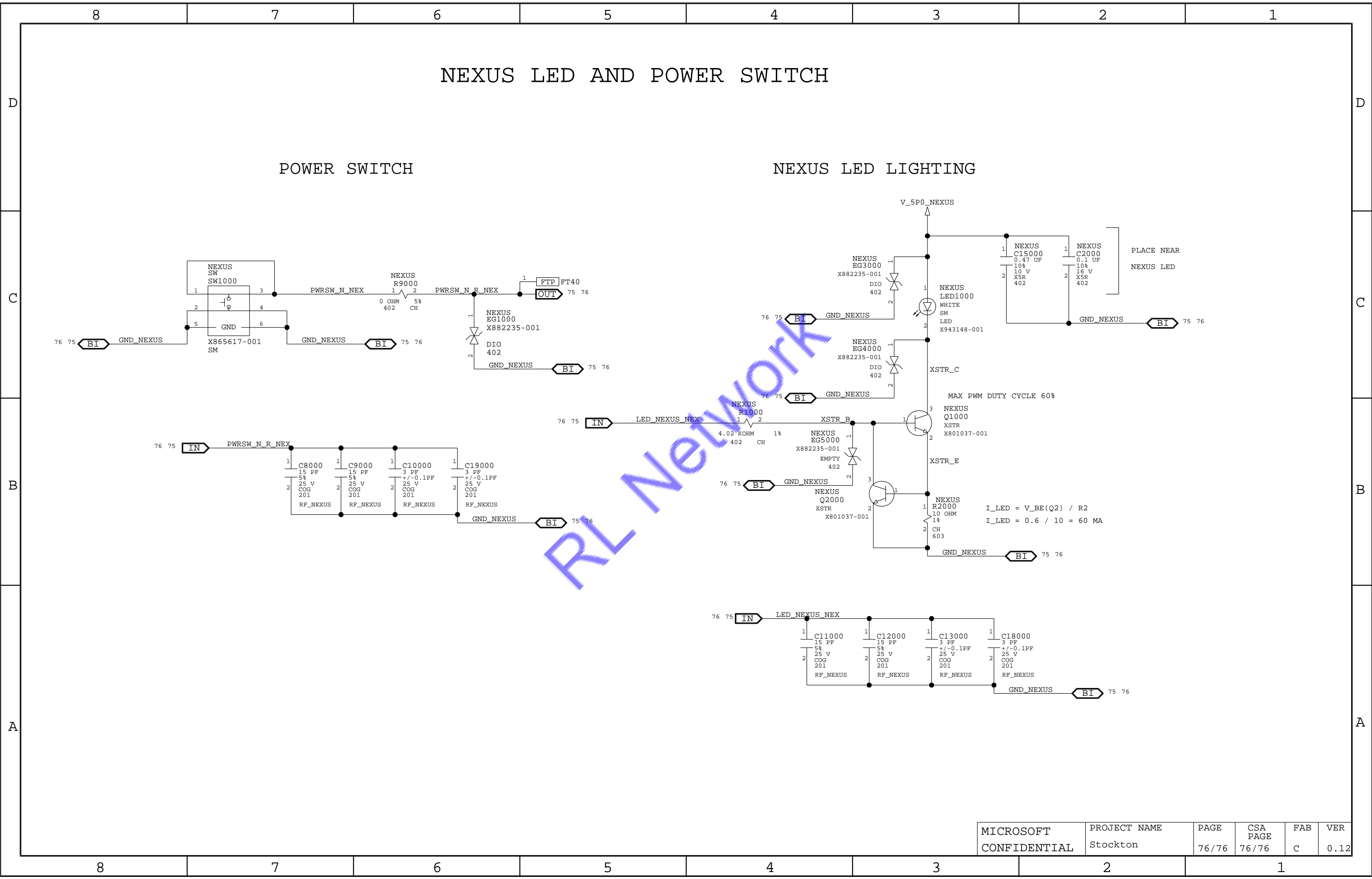
NEXUS BOARD IS CO-PANELED WITH MAIN BOARD

PAGE	CONTENTS
[1]	COVER PAGE
[2]	B2B CONN, LABELS
[3]	NEXUS LED, POWER SWITCH

RL Network

- RULES: (APPLIED WHEN POSSIBLE)
- 1.) MSB TO LSB IS TOP TO BOTTOM
  - 2.) WHEN POSSIBLE: INPUTS ON LEFT, OUTPUTS ON RIGHT
  - 3.) ORDER OF PAGES=CHIP INTERFACES, TERMINATION, POWER, DECOUPLING
  - 4.) AVOID USING OFF PAGE CONNECTORS FOR ON PAGE CONNECTIONS
  - 5.) LANED SIGNALS ARE GROUPED ON SYMBOLS
  - 6.) TRANSIMITTER NAME USED AS PREFIX WITH RX AND TX CONNECTIONS
  - 7.) SUFFIX V\_ IS USED FOR VOLTAGE RAIL SIGNAL NAMES
  - 8.) SUFFIX \_DP AND \_DN ARE USED FOR DIFFERENTIAL PAIRS
  - 9.) UNNAMED NETS ARE NAMED WITH /2 TEXT SIZE
  - 10.) SUFFIX \_N FOR ACTIVE LOW OR N JUNCTION
  - 12.) SUFFIX \_P FOR P JUNCTION
  - 13.) SUFFIX \_EN FOR ENABLE
  - 14.) 'CLK' FOR CLOCKS, 'RST' FOR RESETS
  - 15.) PWRGD FOR POWER GOOD



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